NorthStar™

ADVANTAGE

Technical Manual

00464C

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1.2 SYSTEM DESCRIPTION

The North Star ADVANTAGE is packaged in a molded high impact plastic unit with an integral keyboard. The keyboard features an ASCII typewriter-like layout with programmable function keys and a numeric keypad.

The ADVANTAGE cabinet holds the 12-inch (diagonal) monitor, video circuit assembly, and main processor board which contains the CPU, the memory, the floppy disk controller, the I/O interface circuits, and the power supply regulator. The cabinet also houses either two floppy disk drives or one floppy disk drive and one 5" Winchester hard disk drive.

The ADVANTAGE uses a 4 MHz Z80A microprocessor as the CPU. 64 Kbyte of 200 nsec dynamic random access memory (RAM) is provided for program storage, with a separate 20 Kbyte 200 nsec RAM for the bit-mapped display. A 2 Kbyte PROM contains the resident bootstrap program. An auxiliary 8035 microprocessor controls keyboard and disk input/output (I/O) to and from the CPU.

The display can operate as a 1920 character display with 24 lines x 80 characters or as a bit-mapped display with 240 x 640 pixels. Each pixel is controlled by one bit in the 20 Kbyte display memory.

The n-key rollover keyboard contains 49 standard typewriter keys, 9 symbol or control keys, a 14-key numeric/cursor control pad, and 15 programmable function keys.

In the ADVANTAGE 2Q, the two integral 5-1/4" floppy disk drives are quad capacity double-sided and double-density to provide 360 Kbyte of storage per diskette. In the ADVANTAGE HD-5, the Winchester hard disk drive provides 5 Mbytes of storage.

A simplified block diagram of the ADVANTAGE computer is shown in Figure 1-2. The blocks are described briefly below. Refer to Chapter 4, Theory of Operation for more detailed descriptions of ADVANTAGE component blocks.

- The Central Control Unit maintains primary control of the system. Contained herein are the Z80 and 8035 processors and the controllers for the I/O devices.

- The 64K Main RAM (Random Access Memory) provides temporary storage of programs and data. Programs are executed while residing in this RAM.

- The 2K Boot PROM (Programmable Read-Only Memory) provides bootstrapping and a built-in Mini-Monitor for debugging functions.

- The Video Monitor and 20K Display RAM produce a high resolution display that can be used for graphics applications, or to display messages for the operator.

- The floppy Disk Drive(s) use 5-1/4 inch quad capacity diskettes. The optional hard Disk Drive replaces the second floppy drive.

- The Speaker produces a tone used to signal the operator. The frequency and duration of the tone are under program control.

- The Keyboard includes the standard typewriter configuration, a numeric keypad and 15 programmable function keys.

- The I/O Board Slots allow the ADVANTAGE to be customized for specific applications. There are six board slots which may contain interface boards for external devices or other boards which expand the computing power of the ADVANTAGE. Two types of North Star boards are presently available for use in this area: the Serial Input/Output (SIO) Board and the Parallel Input/Output (PIO) Board. As supplied, the ADVANTAGE contains an SIO board installed in I/O slot one.In an ADVANTAGE HD-5 the Hard Disk Controller resides in I/O slot six.

Functional Block Diagram

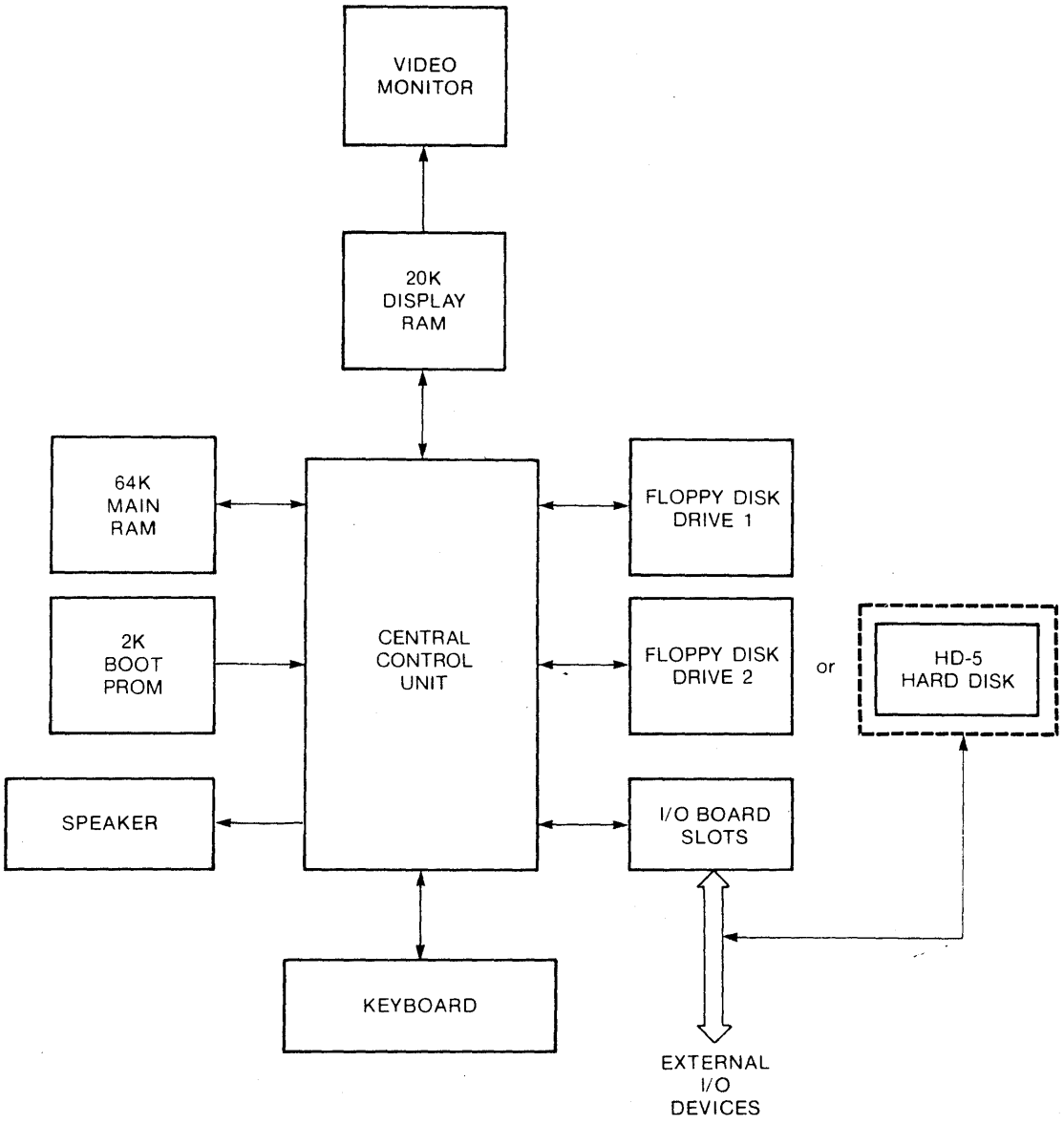


Figure 1-2

1.4 ADVANTAGE SPECIFICATIONS

Table 1-1 lists the physical and electrical characteristics of the ADVANTAGE.

Table 1-1

ADVANTAGE Specifications	
CABINET	
Dimensions	48 cm wide x 51 cm long x 31.5 cm high (18-3/4 in x 20 in x 12-1/2 in)
Net Weight	19.5 kg (43 lbs)
Composition	High impact structural foam
POWER REQUIREMENTS	
External (with Internal Line Filter)	
Domestic	115 VAC, (98 to 132 VAC) 60Hz
International	230 VAC, (196 to 264 VAC) 50/60 Hz
Internal Supply Voltages	±5 VDC ±5% ±12 VDC ±5%
Power Consumption	2 amps @ 115V 1 amp @ 230V
TEMPERATURE AND HUMIDITY	
Operating: (with diskette)	10 C to 40 C (50 F to 104 F) 20% to 80% non-condensing
Non-operating	-40 C to 60 C (-40 F to 140 F)

Table 1-1 (continued)

Shipping	-40 C to 52 C (-40 F to 125 F) 5% to 95% non-condensing
PROCESSOR/MEMORY	
CPU	Z80A Microprocessor, operating speed: 4MHz
	8035 auxiliary processor for keyboard and disk
Memory	64K byte Main RAM 20K byte Display RAM 2K byte Boot PROM
VIDEO	
Screen	28 cm (12 in) diagonal P31 phosphor (green) High impact, non-glare safety shield
Grid	1920 character display, 24 lines by 80 characters
	5X7 character in 8x10 dot matrix
Graphics resolution	240 pixel high x 640 pixel wide
Refresh rate	60 Hz
CRT Anode Voltage	17 KV maximum
KEYBOARD	
Keytops	Sculptured Selectric-compatible N-Key roll-over for fast data entry
Number of Keys:	87
Key Groups	49 Standard Typewriter Keys 14-key Numeric Pad with ENTER key 15 Programmable Function Keys 9 Additional Symbol/Control Keys

Table 1-1 (continued)

Other features	Full Cursor control Special Shift-Lock Keys 5 Shift Modes Auto Repeat

FLOPPY DISK DRIVES

Number of drives	Two floppy disk drives housed in cabinet
Diskettes	Standard 5-1/4 in floppy diskettes. Recommended type: Dysan part No. 107/2D. 512 bytes/sector, 10 (hard) sectors/ track 35 tracks/side, 2 sides/diskette
Storage	Quad (double-sided, double-density) 360K bytes per diskette (formatted)
Transfer Rate	250K bits/second
Latency (average)	100 ms
Access Time Track-to-Track	5 ms
Track Density	48 tpi
Tracks per Side	35

ERROR RATES

Soft errors	1 per 10^8 bits read
Hard errors	1 per 10^{11} bits read
Seek errors	1 per 10^6 seeks
Disk speed	300 rpm $\pm$ 3.0%

Table 1-1 (Continued)

HARD DISK DRIVE

Capacity	
Unformatted	
Per Drive	6.38 megabytes
Per Surface	1.59 megabytes
Per Track	10416 bytes
Formatted	
Per drive	5.0 megabytes
Per surface	1.25 megabytes
Per track	8192 bytes
Per sector	512 bytes
Sectors per track	16
Transfer Rate	5.0 megabits per second
Access Time	
Track to track	3 ms
Average	170 ms
Maximum	500 ms
Settling time	15 ms
Average Latency	8.33 ms
Rotational Speed	3600 rpm ± 1%
Recording Density	7690 bpi max
Flux Density	7690 fci
Track Density	255 tpi
Cylinders	153
Tracks	612
R/W Heads	4
Disks	2

Max Error Rates:

Soft read errors	=	1 per 10^9 bits read
Hard read errors	=	1 per 10^{11} bits read
Seek errors	=	1 per 10^6 seeks

Less bad spots, if any (max 16)
Not recoverable within 16 retries.

Table 1-1 (continued)

INPUT/OUTPUT	
I/O Bus	Slots for up to six plug-in boards (up to five plug-in boards in the HD-5)
	Each board addressed by 16 I/O addresses
Serial I/O (SIO)	RS232 Serial Port
	Current loop option
	Asynchronous: 45 baud to 19.2 kilobaud
	Synchronous: 2400 baud to 51 kilobaud
Parallel I/O	8-bit data in and out with three handshake lines for each port
	Maximum speed is limited by the processor.

This chapter describes startup and general operation of the ADVANTAGE. It contains a description of the keyboard and rear panel controls of the ADVANTAGE. It also provides instructions for loading diskettes in the floppy drive(s), booting a program, and methods for performing a system reset.

2.1 OPERATING CONTROLS

The ADVANTAGE operating controls consist of the keyboard and rear panel controls. On the rear panel are a power switch, screen brightness control, and the system Reset button. For operation of the disk drives, diskette loading and unloading procedures are given.

2.1.1 Keyboard

Primary system control is maintained by entering commands and data from the ADVANTAGE keyboard. The keyboard is illustrated in Figure 2-1. There are 87 keys, described in Table 2-1. The keys generate standard ASCII codes as well as additional 8-bit hex codes. Keys and their codes are listed under various tabulations in Appendix A.

Characters entered from the keyboard are displayed on the CRT screen under program control. A program-maintained cursor marks the position on the screen where the next character entry will be displayed.

The ADVANTAGE Keyboard

Figure 2-1

Table 2-1

ADVANTAGE Keys

Key Group	Keys	Description
CHARACTER	ABCDEFGHIJKLM NOPQRSTUVWXYZ 1234567890!@# $%^&*()-_=+;: '",.<>/?[]{} (space)	Alphabetic, numeric, and special symbols. Numbers and three symbols (.,-) are also available on the numeric pad.
KEYBOARD CONTROL	SHIFT	Either of two identical keys which cause most of the other keys to shift into upper case (see Appendix A).
	ALL CAPS	Shifts only alphabetic characters to upper case. Key is a "push on-off" type with LED to signal when function is active.
	RETURN	Carriage return.
	TAB	Position to next tab set on the line. Setting and releasing tabs is done under program control.
	<X]	Character delete, backspace, or delete and backspace depending upon the program being used.
	ENTER	Numeric pad data entry key.
CURSOR CONTROL	8 direction arrows	All cursor activity is under program control.
	CURSOR LOCK	Shifts only cursor control keys (1-9 on numeric pad) to allow cursor positioning without using SHIFT key. Key is a "push on-push off" type with LED to signal when key is active.

Table 2-1 (continued)

Key Group	Keys	Description
FUNCTION	F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15	Special purpose keys entirely under program control. Each Function key can generate up to three codes.
PROGRAM	ESC	(ESCAPE) key under program control.
	CONTROL	(CTRL) operates as a special shift for keys.
	CMND	(Command) operates as a special shift for keys.

2.1.2 Rear Panel Controls

A rear view of the ADVANTAGE is shown in Figure 2-2. Table 2-2 describes the controls shown in the figure.

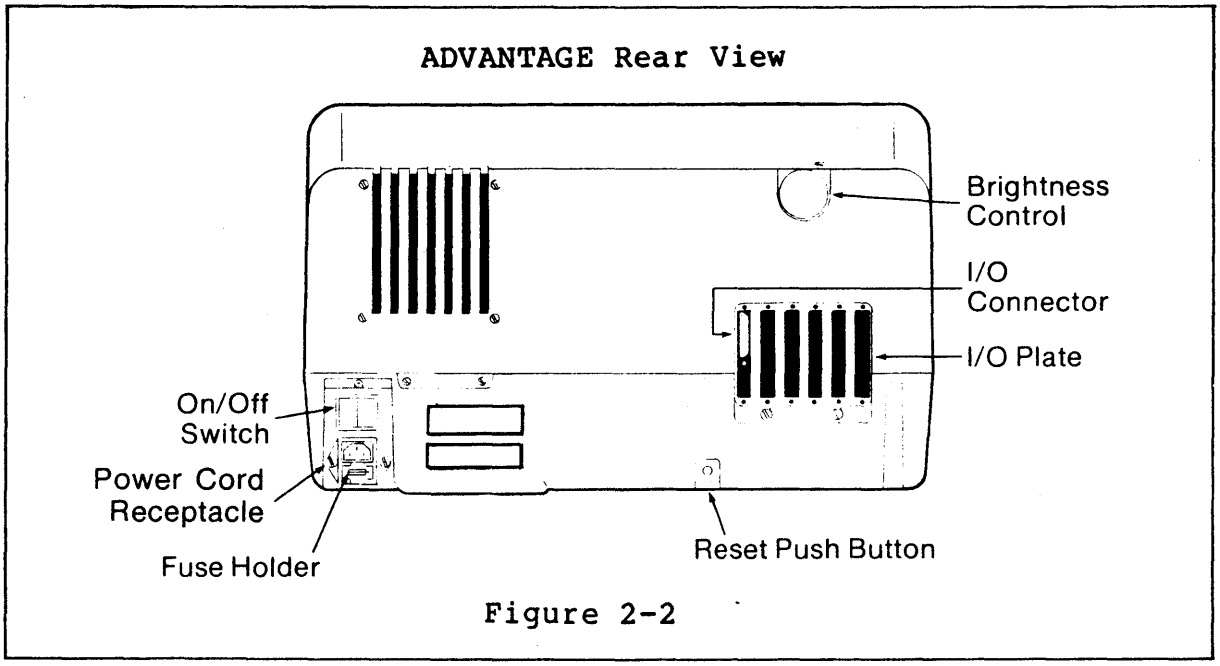


Figure 2-2

Table 2-2

Rear Panel Controls

Control	Description
ON/OFF Switch	Applies/removes electrical power to the unit.
Power Cord Receptacle	Mates with power cord to provide electric current from AC power source.
Fuse Holder	Contains the AC line fuse. Use 2A slo-blo (time delay) fuse for 115V operation and 1A time delay fuse for 230V operation.
Reset Pushbutton	Resets and initializes the system. After reset, data in Main Memory is indeterminate but disk storage data is not affected.
I/O Plate	Openings in plate allow access to I/O connectors on I/O Boards 1 through 6. A Serial I/O Board is a standard installation in slot 1. In hard disk systems, the Hard Disk Controller resides in slot 6.
Brightness Control	Controls brightness of the display screen. Turn clockwise to increase brightness.

2.2 SYSTEM STARTUP

Startup is a function of the bootstrap routines contained in ROM. Drive 1 is programmed as the default drive in the bootstrap program; Drive 1, therefore, is the drive normally used for booting the operating system.

2.2.1 Standard Startup - Booting From Drive 1

To boot from floppy disk drive 1, proceed as follows:

1. Insure that there are no diskettes in the floppy disk drive(s).

CAUTION
Turning power on or off with diskettes loaded may cause loss of data on the diskettes.

2. Turn on ADVANTAGE power by pressing the ON/OFF switch at the rear of the cabinet to the ON position.

3. Insert a system diskette or diagnostic diskette into drive 1. Drive 1 is:

   - the upper drive in an ADVANTAGE with dual floppy drives

   - the lower drive in an ADVANTAGE with a hard disk.

4. Press RETURN after the message "LOAD SYSTEM" appears on the screen. A program is read from drive 1, and control is turned over to the operating system or the diagnostics.

5. Proceed as prompted by the program loaded. If diagnostics have been loaded, refer to Chapter 6 for further information.

2.2.2 Alternate Startup - Booting From Drive 2

An ADVANTAGE with dual floppy drives may be booted from drive 2 (the lower drive). To boot from Drive 2, proceed as in Section 2.2.1, except as follows:

- At step 3 insert the system or diagnostic diskette into Drive 2.
- At step 4 when the "LOAD SYSTEM" message appears, type D2 before pressing RETURN.

2.2.3 Alternate Startup - Booting From A Serial Port

The bootstrap program allows the system to load a program through a serial communication link. To use this feature, you must have a Serial I/O board installed in slot 3. Section 3.13.3 gives details of the communication link.

To boot from a serial port, proceed as follows:

1. Power up the ADVANTAGE (Section 2.2.1) or Reset (Section 2.3) to obtain the "LOAD SYSTEM" message.
2. When the "LOAD SYSTEM" message appears, type S and then press RETURN. The system then boots from the serial port.

2.2.4 Mini-Monitor Startup

The built-in Mini-Monitor may be started up as follows. Refer to Section 6.1 for a description of Mini-Monitor commands:

1. Power up the ADVANTAGE (Section 2.2.1) or Reset (Section 2.3) to obtain the "LOAD SYSTEM" message.
2. When the "LOAD SYSTEM" message appears, press CONTROL-C to enter the Mini-Monitor.

2.3 RESTARTING THE SYSTEM

The ADVANTAGE may be restarted by entering the unique keyboard Reset sequence, by cycling power, or by pushing the rear panel Reset button. Cycling the power forces the CPU program counter to the base address (0000H); the Reset switch and the keyboard sequence both send a non-maskable interrupt (NMI) to the CPU (refer to Section 4.1.1). This interrupt forces the ADVANTAGE to re-initialize and display the "LOAD SYSTEM" prompt.

CAUTION
Resetting the ADVANTAGE during program operation can cause loss of data. Use the keyboard reset feature to reset the ADVANTAGE only to recover from system hard errors. RESET THE ADVANTAGE USING THE REAR PANEL SWITCH ONLY WHEN ALL RECOVERY METHODS HAVE FAILED.

2.3.1 Keyboard Reset

The ADVANTAGE system may be reset by pressing four keys simultaneously on the keyboard. The keys are: CMND, both SHIFT keys, and <X]. The effect of this reset is equivalent to pushing the Reset pushbutton on the rear of the ADVANTAGE cabinet.

The keyboard reset feature may be enabled and disabled under program control. When power is first applied to the ADVANTAGE or after the Reset pushbutton is pressed, the keyboard reset feature is enabled. Thereafter, the feature can be disabled and re-enabled by the program (see Section 3.5.1).

This chapter provides programming information for the various sections of the ADVANTAGE, including the I/O devices. It also explains how to reconfigure the SIO and PIO boards to change their mode of operation.

3.1 MICROPROCESSOR CONTROL

The ADVANTAGE uses the Z-80A microprocessor as its central processing unit (CPU). Refer to the Appendix G for the programming details of this integrated circuit.

3.2 MEMORY CONTROL

3.2.1 Memory Mapping

The ADVANTAGE computer uses a memory mapping scheme to expand its memory addressing capabilities from 64K bytes to 256K bytes. This effectively expands the Memory Address bus from 16 bits to 18 bits.

The addressing scheme divides the 256K bytes into 16 pages of 16K bytes each (see Table 3-1). The three major areas of memory in the ADVANTAGE: the Main RAM, the Display RAM, and the Boot PROM, are permanently assigned to the addresses shown in the table.

Table 3-1

256K Address Space Allocation		
Page	18-Bit Address	Contents
0	00000 - 03FFF	16K bytes of Main RAM
1	04000 - 07FFF	16K bytes of Main RAM
2	08000 - 0BFFF	16K bytes of Main RAM
3	0C000 - 0FFFF	16K bytes of Main RAM
4	10000 - 13FFF	Not presently used
5	14000 - 17FFF	
6	18000 - 1BFFF	
7	1C000 - 1FFFF	
8	20000 - 23FFF	First 16K bytes of Display RAM
9	24000 - 27FFF	Last 4K bytes of Display RAM repeated four times
A	28000 - 2BFFF	Not used
B	2C000 - 2FFFF	Not used
C	30000 - 33FFF	2K-byte Boot PROM repeats to fill 64K bytes
D	34000 - 37FFF	
E	38000 - 3BFFF	
F	3C000 - 3FFFF	

Memory mapping is implemented by four Memory Mapping registers. Figure 3-1 shows how these registers work.

First, output instructions are used to load the register with the appropriate bits. Thereafter, each time the memory is accessed, the upper two bits of the program address automatically generate four bits of memory address by selecting one of the four Memory Mapping registers. The remaining 14 bits of the program address are passed through to the memory address without change.

With any one configuration of the Memory Mapping registers, the program has access to only four of the 16 possible pages. In order to change the four pages it wishes to access, the program must change one or more of the Mapping registers.

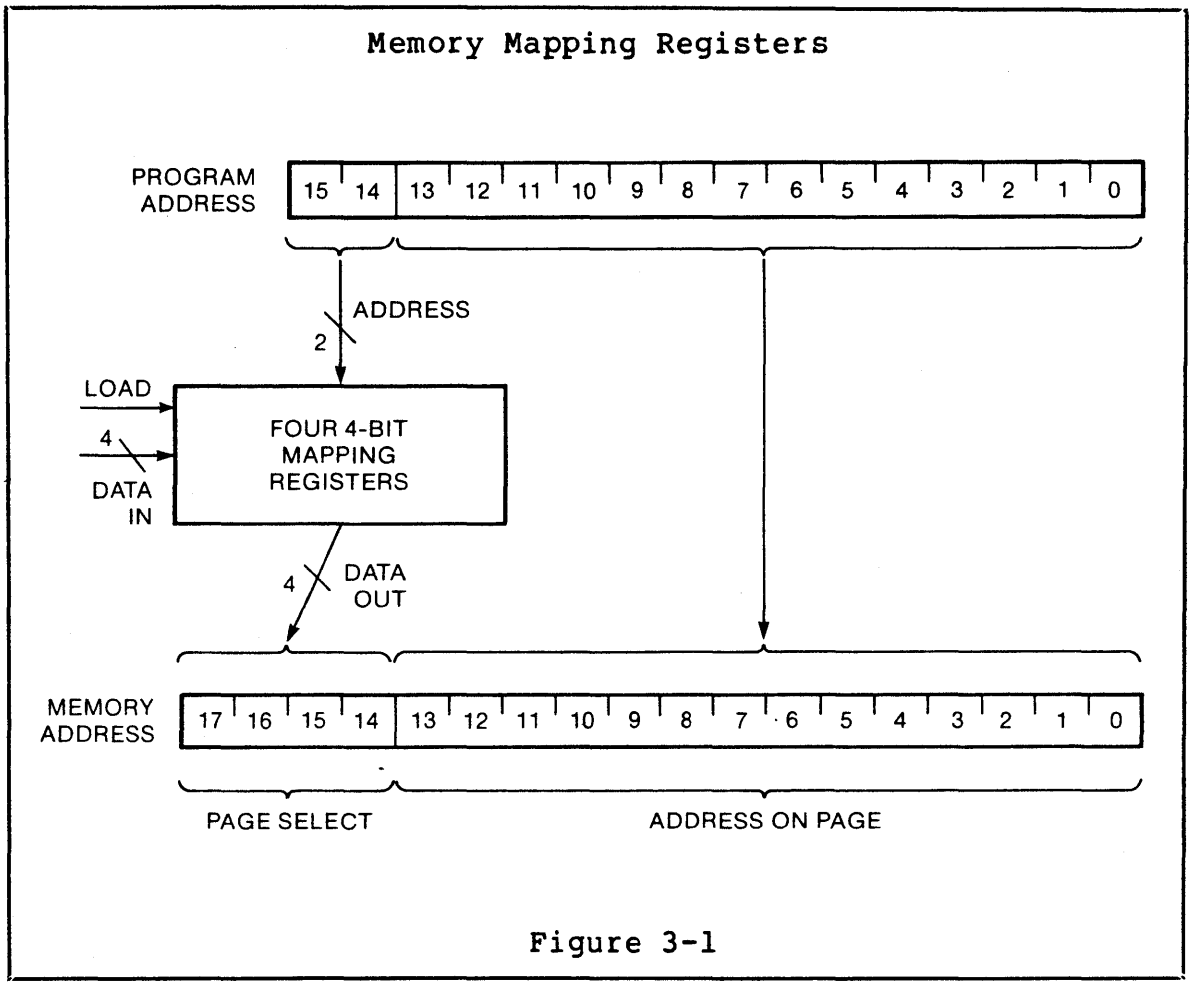

Memory Mapping Registers
PROGRAM ADDRESS
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ADDRESS
2
LOAD
4
DATA IN
FOUR 4-BIT MAPPING REGISTERS
4
DATA OUT
MEMORY ADDRESS
17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
PAGE SELECT
ADDRESS ON PAGE

Figure 3-1

Table 3-10 (Continued)

NOTES

- Bits 0-3 are only valid after bit 7 changes state to acknowledge that the command has been executed.
- When bits 0-3 contain the disk sector number, they have a range of 0-9 for the 10 sectors, or one of the following special codes:

  E = disk drive motors off
  F = index pulse detected

3.5 KEYBOARD CONTROL

This section contains the programming information for the ADVANTAGE keyboard. Refer to the diagrams and tables in Section 3.4 for the following discussion.

3.5.1 Keyboard Reset Enable

The 4-key reset feature of the ADVANTAGE keyboard may be enabled or disabled under program control. This feature is initially enabled at power-up. It may be disabled under program control by issuing the two-command sequence "6,7" to the I/O Control register (I/O address F0H) when the feature is enabled. This command sequence complements the current state of the Keyboard NMI flag and places its current state into bit 0 of I/O Status register 2 (I/O address D0H).

The keyboard reset is enabled by power-on reset, pushing the RESET button, or by the program issuing the "6,7" sequence to the I/O Control register when the feature is disabled. Once enabled, the 4-key keyboard reset functions exactly like the RESET pushbutton reset. It forces a non-maskable interrupt to reset the system as described in the following section.

3. Wait for the Command Acknowledge bit to complement. This delay is in the range of 0.5 to 1.5 milliseconds.

4. Input from I/O Status register 2 and check bit 0. If this bit is on, the KB MI flag is now set.

5. If the KB MI flag is reset, repeat step 2 above.

When the keyboard causes an interrupt, the program can verify the source of the interrupt by inputting from I/O Status register and checking bit 0. This bit is on if the keyboard is interrupting.

To clear the interrupt, the program must input keyboard characters (see Section 3.5.4) until the Keyboard Data flag is reset. This flag is bit 6 of I/O Status register 2.

Polled. If the keyboard is to be polled rather than operated in interrupt mode, the KB MI flag must be reset. This flag is reset when the ADVANTAGE power is turned on, or when the ADVANTAGE Reset Button is pushed. The program may reset the KB MI flag by repeating the same sequence as above and checking the bit for "off" (zero) at step 4. Perform a repeat (step 5) if the KB MI flag is set.

The program polls the keyboard by periodically inputting from I/O Status register 2 (I/O address D0H) and checking bit 6. If the bit is on, the program reads the keyboard character(s) as described below.

3.7 FLOPPY DISK DRIVE CONTROL

The Floppy Disk Drive Controller uses a minimum of hardware and requires a sophisticated program, implemented in ROM, to read from and write to the disk drives. Some of the timing and motor control is determined by the program.

The program communicates with the Floppy Disk Controller in the following ways:

1. Through the Shared I/O Interface registers described in Section 3.4.

2. By outputting control bytes to the Drive Control register. The format for the register is shown in Table 3-16, and its I/O address is listed in Table 3-15.

3. By accessing the other I/O addresses given in Table 3-15.

Table 3-15

Floppy Disk I/O Addresses

I/O Address (Hexadecimal)	Operation	Description
80	INPUT	Input Disk Data. Sets the processor into the wait state until the disk data is available, then reads the data. Inputting from this address when data is unavailable puts the processor into a continuous wait state.
80	OUTPUT	Output Disk Data. Sets the processor into the wait state until the Disk Controller writes the data to the diskette. Outputting to this address before setting the Disk Write flag puts the processor into a continuous wait state.

Table 3-15 (continued)

81	INPUT	Input Sync Byte. Sets the processor into the wait state until the sync byte is available, then reads the data. If the disk format is correct, the character read is a BFH. Inputting from this address when a sync byte is not available puts the processor into a continuous wait state.
81	OUTPUT	Load Drive Control Register. See Table 3-16 for the register format.
82	INPUT	Clear Disk Read Flag. Terminates the disk read operation. The data input by this address is indeterminate.
82	OUTPUT	Set Disk Read Flag. This flag is set as one of the steps in initiating a disk read operation. The output data is ignored.
83	OUTPUT	Set Data Write Flag. This flag is set to initiate a disk write operation. The output data is ignored. The Disk Write flag is cleared on the leading edge of the next sector mark.

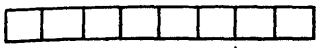
NOTES

- When these I/O addresses are decoded, bits 2 and 3 are ignored. This produces four address for each function that work equally well. For example, addresses 80, 84, 88 and 8C all produce identical results.
- If a disk operation causes the processor to go into a continuous wait state, the Main RAM refresh cycles are interrupted and data in Main RAM is lost.

Table 3-16

Floppy Drive Control Register Format

I/O Address 81H (output only)



Disk Drive 1. A one selects disk drive 1. Bit 1 must be off.

Disk Drive 2. A one selects disk drive 2. Bit 0 must be off. This bit is not used in the ADVANTAGE HD-5 floppy drive.

Not used.

Step Pulse. Setting this bit on, then resetting it, causes the head to step in the selected disk drive. This bit must remain off for at least 5 milliseconds between step pulses.

Step Direction/Precompensation

A. During stepping of the disk from track to track, this bit determines the step direction.
   0 = Step toward outer cylinder
   1 = Step toward inner cylinder

B. During writing, this bit controls write precompensation.
   1 = Use precompensation
   0 = Use no precompensation.

Precompensation is required on the inside 20 cylinders- tracks 15 through 34 on side 0 and tracks 35 through 49 on side 1.

Diskette Side Select.
   0 = Side 0
   1 = Side 1

Not used

A disk operation involves selecting the drive, enabling the motor, performing a head seek, selecting a sector, and then performing the read or write operation. These operations are described separately in the following subsections.

3.7.1 Power-On Initialization

The data separation circuitry must be initialized after power is applied to the disk controller but before a read or write operation. This is done by alternately setting and clearing the Disk Read flag (I/O address 82H)) at approximately 100-millisecond intervals for five cycles.

3.7.2 Motor Enable

Both disk drive motors are turned on whenever a command 5 is received (Start Disk Drive Motors, see Table 3-8). If the command 5 is removed for three seconds, the value 0EH is displayed as the sector number. After 100 microseconds both disk drive motors are turned off and the Drive Control register is reset to zeros. The 100-microsecond delay prevents the motors from being turned off in the middle of a read or write operation.

3.7.3 Drive Selection

After the drive motors are turned on, the program loads the Drive Control register (see Table 3-16) to select one of the two drives. In the ADVANTAGE HD-5, this drive is always disk drive 1, i.e., the floppy drive. At the same time the other bits of the register may be loaded in preparation for a head seek, read, or write.

3.7.4 Seek

The positioning of the disk drive read/write head is entirely under program control. The program must keep track of the position of the head and generate the timing pulses required to move the head from track to track.

The head is initialized (set on Track 0) by stepping it one track at a time toward the outside of the diskette, and after each step, inputting I/O Status register 1 (I/O address E0H). Bit 5 of the register is on when the selected drive has its head positioned on track 0. There are 35 tracks per side.

The head is stepped by setting and then resetting bit 4 of the Drive Control register (I/O address 81H). When the head is moved by more than one track in either direction, this bit must remain off for at least 5 milliseconds between step pulses. When the head reaches its destination, the program must delay at least 20 milliseconds to allow time for the head to settle.

3.7.5 Sector Selection

The sector number is read by performing the following sequence:

1. Input and record the state of the Command Acknowledge bit (I/O address D0H, bit 7).

2. Issue command 5 to the I/O Control register (I/O address F0H, refer to section 3.4).

3. Wait for the command acknowledge bit to complement. This delay is in the range of 0.5 to 1.5 milliseconds.

4. Input the Sector Mark bit (I/O address E0H, bit 6) until it is found to be zero.

5. Input the sector number (I/O address D0H, bits 0 through 3). This number is valid while the Sector bit is zero, and for 50 microseconds thereafter.

The number obtained by following the above procedure is actually the number of the previous sector. For example, if sector 6 is to be accessed, the program must search for sector 5. If the desired sector is not found on the first attempt, repeat steps 4 and 5 above until it is found.

When the correct sector has been located, the program goes into a loop, waiting for the sector mark to go from a zero to a one. The read or write operation sequence must be initiated on this transition.

3.7.6 Read Data

After the proper sector number is found, the read sequence is as follows:

1. Wait 500 microseconds after the zero-to-one transition of the Sector Mark bit.

2. Set the Disk Read flag by outputting to I/O address 82H.

3. Change the Acquire Mode flag to zero (bit 3 of I/O address F0H).

4. Wait 150 microseconds, then change the Acquire Mode flag to a one.

5. Wait until the Disk Serial Data bit (I/O address E0H, bit 7) changes to a one.

6. Input the sync byte (I/O address 81H). This byte should be FBH.

7. Input from I/O address 80H for the remainder of the data. The next byte read is the second sync byte, which is (sector number) + (16 x track number) truncated to the lower eight bits. Following this are the 512 data bytes and the CRC byte. The CRC byte is not checked by hardware; a software routine is needed if checking is desired.

8. The program's task is complete at this point. The hardware will reset the Disk Read flag at the zero-to-one edge of the next sector mark. During the sector mark a new read sequence can be started.

Read timing is illustrated in Figure 3-4A. Note that the timing is such that consecutive sectors may be read.

3.7.7 Write Data

After the proper sector number is found, the write sequence is as follows:

1. Input the Write Protect bit (I/O address E0H, bit 4). The bit must be a zero to write on the diskette.

2. If writing to one of the inner tracks, set the Precompensation bit (I/O address 81H, bit 5). Precompensation is required on tracks 15 through 34 on side 0, and tracks 35 through 49 on side 1.

3. Set the Disk Write flag by outputting to I/O address 83H. This must be done within 150 microseconds after the zero-to-one transition of the Sector Mark bit (I/O address E0H, bit 6).

4. Output 33 consecutive bytes of zeros to I/O address 80H. This forms the preamble of the sector.

5. Output two sync bytes to I/O address 80H. The first contains the synchronization byte (0FBH), and the second contains the sector address (see READ DATA).

6. Output 512 data bytes to I/O address 80H.

7. Output the CRC byte to I/O address 80H. Note that the program must calculate the CRC byte.

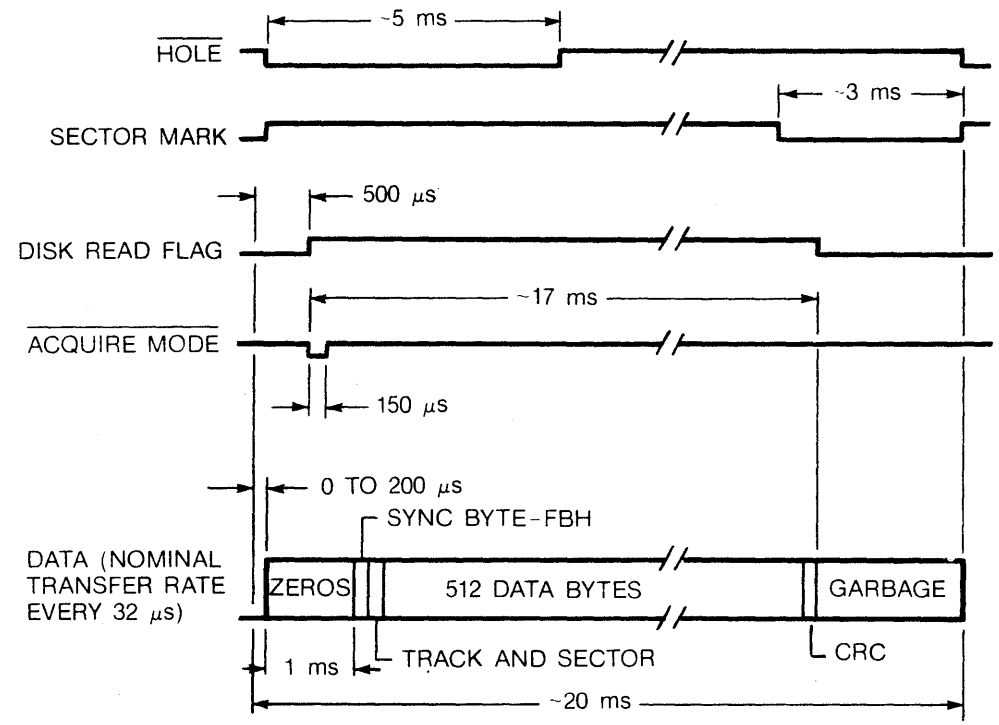
8. The program's task is complete at this point. The hardware will reset the Disk Write flag at the zero-to-one edge of the next sector mark. During the sector mark a new write sequence can be started.

Note that it is possible to write contiguous sectors by waiting for the Sector Mark bit to return to zero, and starting again with step 3 above.

Write timing is illustrated in Figure 3-4B.

Disk Read/Write Timing

A-READ TIMING



B-WRITE TIMING

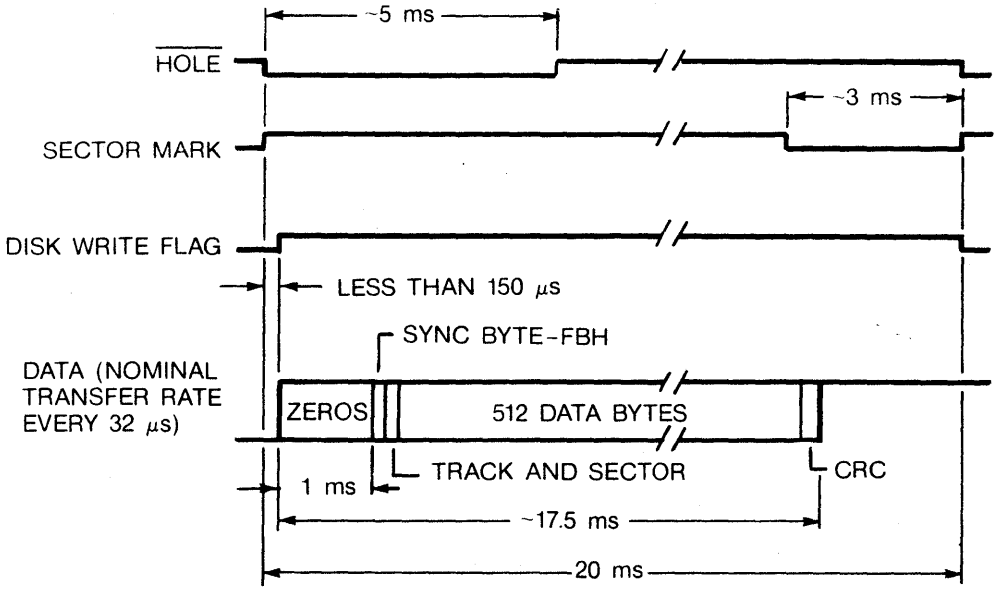


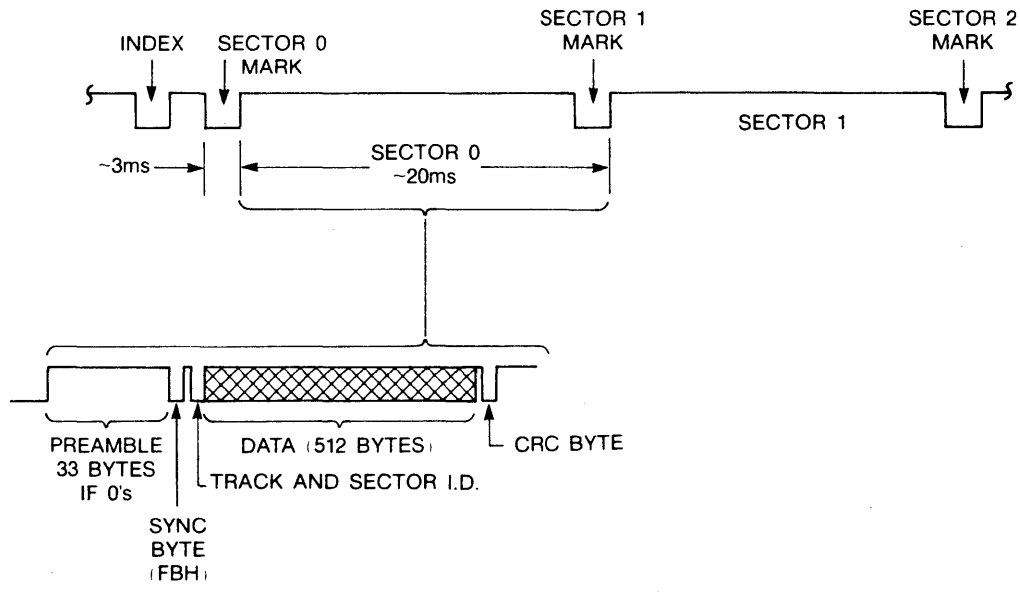
Figure 3-4

3.7.8 Floppy Disk Data Format

Each floppy disk is formatted for 35 data tracks per side, with each track containing 10 hard sectors. Index holes in the diskette media physically mark the beginning of each sector. An eleventh index hole provides the Floppy Disk Controller with an indication of one complete disk revolution. Actual disk recording begins approximately 96 microseconds after sector hole detection.

The data format is shown in Figure 3-5. Each sector contains a Preamble (16 bytes of zeros), a Sync Character (FBH) byte, 256 bytes of data, and a Check Character byte. The formatting program computes the Check Character constantly by setting it to zero, then exclusive ORing each successive data byte value with the current value of the Check Character and rotating the byte left one bit.

Floppy Disk Track and Sector Format



NOTE: WAVEFORMS REPRESENTATIVE OF DATA SEPARATOR OUTPUT (DATA POSITIVE TRUE, ALL ELSE NEGATIVE TRUE)

Figure 3-5

3.8 HARD DISK DRIVE CONTROL

The ADVANTAGE HD-5 has a separate Disk Controller board dedicated to the hard disk.

It requires its own disk driver program to perform read or write operations. The driver program must:

- Format the drive.
- Position the drive head over the desired track
- Locate the desired data sector.
- Initiate the read or write operation.

These operations are described in detail in this section.

The program communicates with the controller through 16 contiguous I/O ports (addresses). Although only eight of the addresses are used in performing a read or write operation, the controller responds to all 16. Commands used to communicate with the controller via the I/O ports are described in Section 3.8.1.

3.8.1 I/O Commands

The controller occupies an address space of 16 consecutive I/O addresses. The controller responds to eight input commands and three output commands, as described in Table 3-17.

Table 3-17

Hard Disk Drive I/O Commands

I/O Address (Hexadecimal)	Function
OUTPUT COMMANDS	
05	Load Sector Counter. Loads the Sector Counter in the controller. This command is used only when formatting the disk drive to write the controller index pulse. It prevents an inadvertent sector pulse from stopping the write operation when the drive is being formatted.
06	Load Control Register. Loads the Drive Control register in the controller. The control bits are defined in Table 3-18.
07	Host Write RAM. Writes the data into the RAM location to which the RAM Address Counter currently points. The RAM Address Counter is incremented by 1 after the RAM write is complete.
INPUT COMMANDS	
00	Read RAM. Reads the data from the RAM location to which the RAM Address Counter currently points. At the end of the input operation, the RAM Address Counter is incremented by 1.
01	Read Status. Transfers information from the Controller Status register to the computer. The status bits are defined in Table 3-19.

Table 3-17 (Continued)

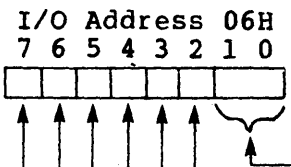
I/O Address (Hexadecimal)	Function
02	Clear RAM Address. Resets the RAM Address Counter to location 0.
03	Clear Sector. Clears the sector pulse latch.
04	Start Sync. Sets the enable sync latch. This latch is set at the beginning of each read to allow the controller board to synchronize with the preamble at the beginning of the sector (see Figure 3-6).
05	Start Read. Sets the read enable flip-flop and clears the sync latch. This allows the controller to begin looking for the sector sync byte.
06	Start Write. Sets the write latch in the controller, enabling writing on the drive.
07	Format Write. Sets the write latch and clears the index one-shot. This command is used only when formatting the drive to permit writing during the index pulse.

NOTE

In decoding the I/O address, the controller ignores bit 3. Thus, for each function, there are two addresses that work equally well: Addresses 00 and 08 produce identical results, as do 01 and 09, 02 and 0A, etc. In this table only the nominal form (bit 3=0) is listed.

Table 3-18

Hard Disk Drive Control Register Format



Head Select. Binary code selects one of four drive heads (numbered 0 through 3).

Reserved for future use.

Low Write Current. Controls the reduced write current signal to the drive. This bit must be set to:

0 = for writing on cylinders 0 through 127 (normal current).

1 = for writing on cylinders 128 through 152 (low current).

Head Step Pulse. This bit must be set to one and then zero under program control to issue a head step pulse to the drive.

Step Direction/Precompensation.

A. During stepping of the heads from cylinder to cylinder, this bit determines the step direction:
   0 = Step toward inner cylinder (higher number cylinder).
   1 = Step toward outer cylinder (lower number cylinder).

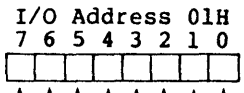
B. During writing, this bit controls write precompensation:
   0 = precompensation on
   1 = precompensation off
   Precompensation is required on cylinders 64 through 152.

Not used.

Header Read Enable. When set to a one, this bit causes the controller to read the first 15 bytes of a sector into controller RAM locations 1 through 15. This implies that the Clear RAM Address command (input, I/O address 02H) was executed before executing the read operation, so that the RAM address starts at zero.

Table 3-19

Hard Disk Controller/Drive Status Bits



Write Fault. A zero indicates that there is a fault in the drive and that it is not safe to perform any operations with the drive.

Seek Complete. A zero indicates that the seek is complete in a drive and that all head motion has stopped. This bit, in conjunction with the Drive Selected and Ready bits (3 and 4, respectively) is used to determine when a drive is ready to read and write.

Track 0. A zero indicates that the drive head is positioned over cylinder 0.

Drive Selected. A zero indicates that the drive is selected. The drive is automatically selected as soon as power is applied to the drive and remains a zero as long as the drive is selected.

Ready. A zero indicates that the drive is ready for a new operation. This bit becomes a zero approximately 15 seconds after power is applied to the drive and remains a zero as long as the drive is selected.

Read/Write Active. A one indicates that the controller is in the process of performing a read or write operation. During these times no access by the program is permitted to the controller RAM memory. This bit is asserted when the actual input sync byte has been found on read and remains asserted until the next sector pulse. For a write operation, the bit is asserted when the Start Write command (input, I/O address 06H) is executed and remains asserted until the next sector pulse.

Controller Index. A zero indicates that the controller index pulse is present. This bit goes low on the leading edge of the physical index pulse from the drive and returns high when the controller's index pulse written on the data track is detected. The bit is guaranteed to be low for a minimum of 100 microseconds per revolution.

Controller Sector. A one indicates that the controller has seen a sector pulse. This bit is the output of a latch that is set each time the electronically generated sector pulse occurs. It is cleared under program control, using the Clear Sector command (input, I/O address 03H). Note that the first sector pulse is generated immediately after the index pulse.

3.8.2 Head Positioning

Positioning of the head over the respective cylinders is entirely under program control. The hard disk drive has 153 cylinders. Positioning from cylinder to cylinder is performed by a stepper motor (as in the floppy disk drive). The program is required to maintain the current cylinder number within the software and to determine the direction and number of tracks to move to get to a new track.

A bad spot table is maintained on track 0. Bad spots are tracks on which one or more sectors have proven to be unreliable in factory testing. Bad spots are also listed on the HD-5 Bad Spot Label located on the side of the disk drive. The program does not use tracks that have been designated as bad spots.

Track 0 Sensing

The operation begins by sensing whether or not the disk drive is presently located over track 0 (Input, I/O address 01H, bit 2). If it is, the drive is stepped inward until the track 0 bit changes to a one.

This feature guards against the situation where the head has moved itself outside track 0 and is on a negative numbered track. The number of steps permitted in this inward direction is 20, which should ensure that the drive is not inside track 0. If it takes more than 20 steps, the drive is faulty.

Once the track 0 bit changes to a one, or if it was initially a one, the head is stepped towards the outside of the drive one step at a time until the track 0 bit changes again to a zero, showing that the head is located over track 0. If more than 153 track movements do not cause the track 0 indication to become true, the drive is faulty.

3.10 SIO BOARD

The Serial Input/Output (SIO) Board provides a general facility for communicating with serial I/O devices. Synchronous and asynchronous operation are described in separate subsections. This section begins by describing those features of the board that are common to both synchronous and asynchronous operation.

3.10.1 Reset

When the I/O Reset bit (I/O address F0H, bit 4) is set on, then off, it has the following effect on the SIO Board:

1. The Interrupt Mask is cleared to zeros, preventing any interrupts from the board.

2. The Baud Rate register is cleared to zeros. Normally the register would now have to be reloaded to select the desired baud rate. See the appropriate section below.

3. The USART is reset, in preparation for reprogramming.

Note that the I/O Reset bit resets all I/O Boards simultaneously.

3.10.2 Board ID

The 8-bit identification code for the SIO Board is F7H. The I/O address used to input this code is determined by the board slot occupied by the SIO (see Table 3-20).

3.10.3 Data Transfers

The I/O address used to transfer a data byte to or from the SIO Board is x0H, where x is determined by the board slot occupied by the SIO (see Table 3-22). The standard location for the SIO Board is slot 1.

Table 3-22

First Digit of I/O Address	
Board Slot	First Digit of I/O Address
6	0
5	1
4	2
3	3
2	4
1	5

3.10.4 Control

The operation of the SIO Board is controlled by specifying the Interrupt Mask and the baud rate, and by programming the 8251 USART IC (integrated circuit).

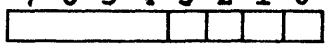
The format of the Interrupt Mask is shown in Table 3-23. A one in any of the bit positions 0 through 3 allows the SIO Board to generate a maskable interrupt if the stated condition occurs. The program defines this mask by outputting the appropriate bit pattern to I/O address xAH, where x is determined by the board slot occupied by the SIO Board (see Table 3-22).

The baud rate is specified by loading the Baud Rate register as described in the appropriate section: 3.10.7 for asynchronous mode, and 3.10.8 for synchronous mode.

Table 3-23

SIO Interrupt Mask Format

I/O Address xAH where x = 0 - 5



Tx Empty. Transmitter has finished sending characters.

Tx Ready. Buffer is ready to receive the next character.

Rx Ready. Receiver has a character ready.

Sync Detect. Synchronization has been achieved (synchronous mode only).

Unused.

NOTE: A one in any bit position 0 through 3 allows the stated condition to generate a maskable interrupt.

Programming the 8251 USART is done by resetting the SIO Board (see Section 3.10.1), then outputting a series of control bytes to the SIO. These bytes are output to I/O address x1H, where x depends upon the board slot occupied by the SIO Board. The control bytes necessary to configure the SIO for a particular mode of operation such as synchronous/asynchronous, number of bits per character, etc., are defined in the specification sheets for this IC, which can be found in Appendix H.

3.10.5 Status

A status byte may be read from the SIO Board by inputting I/O address x1H, where x depends upon the board slot occupied by the SIO Board (see Table 3-22). The composition of this status byte is given in the specification sheets for the 8251 USART, which can be found in Appendix H.

Table 3-24

Serial I/O Addresses

I/O Address (Hexadecimal)	Operation	Description
X0	INPUT/OUTPUT	USART data
X1	INPUT/OUTPUT	USART Status/Command
X8	OUTPUT	Baud Rate Register
XA	OUTPUT	Interrupt Mask

NOTES

- The first digit of these I/O addresses is determined by the board slot occupied by the SIO board (see Table 3-22).
- The Baud Rate register may also be accessed by using I/O address x9.
- The Interrupt Mask may also be accessed by using I/O address xB.
- Inputting from I/O addresses x8, x9, xA or xB causes indeterminate data to be loaded.

3.10.6 Interrupt or Polled

The SIO Board may be serviced in the interrupt mode or it may be polled by the program.

If the interrupt mode is used, one or more bits of the Interrupt Mask must be set to allow the USART to generate interrupts. The Interrupt Mask is discussed in Section 3.10.4.

When the SIO Board causes an interrupt, the program must determine the source of the interrupt. It does this by inputting from I/O address E0H and checking bit 1. The bit is a zero if any of the I/O boards including the SIO are interrupting. The program then inputs the status of all I/O boards to determine which board(s) is interrupting.

The program decides whether the SIO board has interrupted by comparing the status bits to the bits in the Interrupt Mask. The program can respond by inputting or outputting a data byte, as appropriate, or by simply masking the interrupting condition.

If the SIO Board is to be polled, the Interrupt Mask must be loaded with zeros. The program polls the SIO by periodically reading the status byte from the 8251 USART (see Section 3.10.5) and taking appropriate action.

3.10.7 SIO in Asynchronous Mode

A. Asynchronous Modem Configuration

To establish a communication link between two electronic devices, one device must simulate a modem while the other simulates a terminal. If the ADVANTAGE is to communicate with a serial terminal such as an external CRT, a teletype, or a serial printer, the SIO must be configured to simulate a modem. Similarly, if the ADVANTAGE is to communicate with a modem, the SIO must simulate a terminal.

As shipped, the SIO is configured as a modem; it is ready for immediate connection to an asynchronous RS-232 terminal or a North Star-supplied printer. Connection to most asynchronous terminals and printers requires no configuration changes.

If the SIO has ever been reconfigured as a terminal, it can be restored to its original configuration as follows:

1. Remove the Clock Header in board location 1A, if one is present.

2. Remove the Configuration Header, board location 3A, and replace it with a 16-pin header wired as shown in Figure 3-7.

Asynchronous Modem Configuration Header

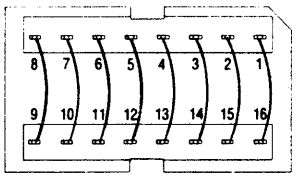


Figure 3-7

B. Asynchronous Terminal Configuration

If the ADVANTAGE is to communicate with a modem (or with another computer simulating a modem) the interfacing SIO port must be configured to simulate a terminal.

To configure the SIO as a terminal, proceed as follows:

1. Remove the Clock Header in board location 1A, if one is present.

2. Remove the Configuration Header from board location 3A and replace it with a 16-pin header wired as shown in Figure 3-8.

Asynchronous Terminal Configuration Header

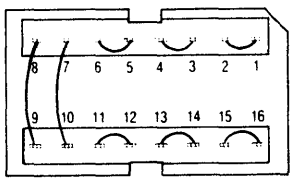


Figure 3-8

C. Current Loop Operation

Whereas most computers, terminals, and printers use RS-232 signal levels, some terminals, such as teletypes, use 20 mA current loop signals.

A teletype is a passive device; it does not supply current, but relies on current supplied by the SIO. The SIO is not equipped to accommodate active current loop devices such as computers that produce current loop signals.

As shipped, each SIO board is configured to use RS-232 signals.

To configure an SIO for current loop operation, perform the following procedure:

1. Remove the Configuration Header, board location 3A, and replace it with a 16-pin header wired as shown in Figure 3-9.

Current Loop Configuration Header

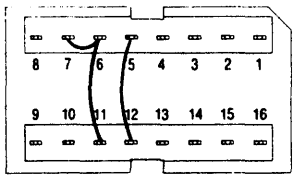


Figure 3-9

2. Remove the 1488 in location 4A and replace it with the Current Loop circuit built on a 14-pin header. This circuit is shown in Figure 3-10 and is constructed as follows:

   a. Connect a 2N3904 transistor to the 14-pin header with the emitter (E) lead connected to pin 7, the base (B) lead connected to pin 5 and the collector (C) lead connected to pin 6.

   b. Solder a 5.6K ohm 1/4 Watt resistor between pin 4 and pin 12 on the header.

   c. Solder a 1K ohm 1/4 Watt resistor between pin 8 and pin 14 on the header.

Current Loop Circuit

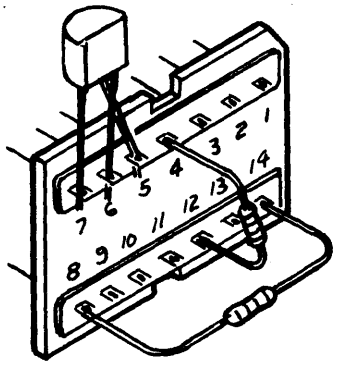


Figure 3-10

3. Connect a 25-pin D-type connector to the terminal cable as follows:

   pin 9 to the printer +lead
   pin 3 to the printer -lead
   pin 2 to the keyboard +lead
   pin 10 to the keyboard -lead

The procedure is then complete.

D. Asynchronous Printers

As noted earlier, most asynchronous printers can be connected to the SIO with no configuration changes. For a few printers, however, the buffer full status signal may be on an alternate pin.

The SIO supports printers that indicate buffer full status on Pin 20 (DTR) or on pin 19 (SCA). Consult the manual for your printer to determine which pin is used to indicate buffer full status. Depending on the manufacturer, this signal may be identified as "Printer Ready" or "Buffer Full."

As shipped, the SIO expects the buffer full signal on pin 20. If this signal is on pin 19, the SIO Board must be modified as shown in Figure 3-11.

Buffer Full Modification

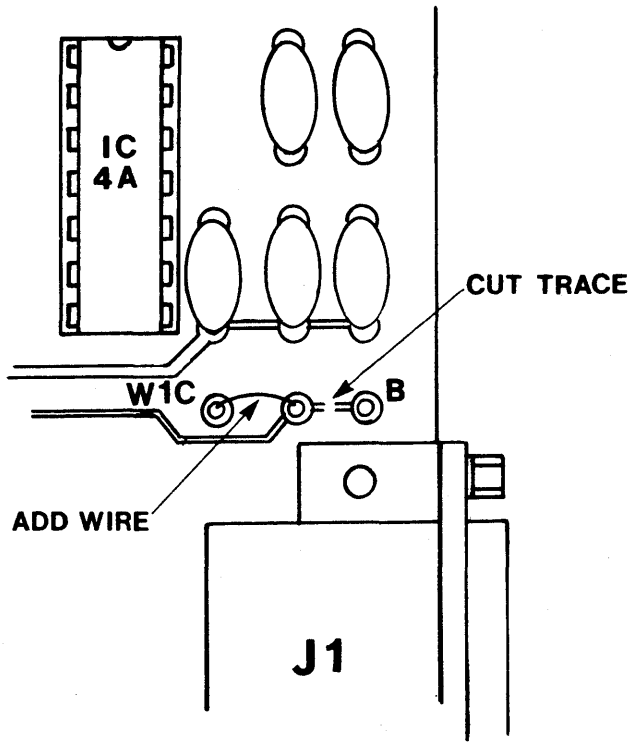


Figure 3-11

E. Asynchronous Baud Rate Selection

The baud rate is selected by a combination of the USART command to "divide by 16" or to "divide by 64" and the value placed in the Baud Rate register. This register is loaded via I/O address x8H, where x is determined by the board slot occupied by the SIO board (see Table 3-22). Table 3-25 shows the values that produce the commonly used baud rates.

Table 3-25

Asynchronous Baud Rate Selection

Baud Rate	USART set to ÷ 16 Baud Rate Register		USART set to ÷ 64 Baud Rate Register	
	Decimal	Hexadecimal	Decimal	Hexadecimal
19200	127	7F	--	--
9600	126	7E	--	--
4800	124	7C	127	7F
2400	120	78	126	7E
1200	112	70	124	7C
600	96	60	120	78
300	64	40	112	70
200	32	20	104	68
150	0	00	96	60
110	--	--	84	54
75	--	--	64	40
50	--	--	32	20
45	--	--	22	16

F. Asynchronous Programming Examples

Table 3-26 illustrates a method of programming the SIO Board for asynchronous operation.

Table 3-26

Sample Asynchronous I/O Routines for SIO Board

```
0000                ;
0000                ;
0030                PORTA   EQU     30H     ; Set for SIO boardlet in slot three.
0038                BAUD    EQU     PORTA+8 ; Set Baud rate for channel
0030                DATA    EQU     PORTA   ; USART data address
0031                CTRL    EQU     PORTA+1 ; USART control/status.
007F                BDRT    EQU     127     ; Set Baud rate of 19.2K Baud
0000                ;
0000                ;
0000                ;
0000                ;               Input and output routines
0000                ;
0000  DB31          CINA    IN      CTRL            ; Check USART status
0002  E602                  ANI     2               ; Get RxReady bit
0004  28FA                  JRZ     CINA            ; Wait till character ready
0006  DB30                  IN      DATA            ; Read character
0008  E67F                  ANI     7FH             ; Mask off top bit
000A  C9                    RET
000B                ;
000B  DB31          COUTA   IN      CTRL            ; Check USART status
000D  E601                  ANI     1               ; Get TxReady bit
000F  28FA                  JRZ     COUTA           ; Wait till ready
0011  78                    MOV     A,B             ; Output char is in B reg
0012  D330                  OUT     DATA            ; Output character
0014  C9                    RET
0015                ;
0015                ;  SIO Boardlet initialization routine
0015                ;
0015  3E7F          INIT    MVI     A,BDRT
0017  D338                  OUT     BAUD            ; Set baud rate
0019                ;
0019                ;  Interrupt masks are cleared at power up
0019                ;
0019  3E03                  MVI     A,3             ; Give USART commands
001B  D331                  OUT     CTRL            ; to reset.
001D  D331                  OUT     CTRL
001F  3E40                  MVI     A,40H
0021  D331                  OUT     CTRL
0023  3ECE                  MVI     A,0CEH          ; Give mode command
0025  D331                  OUT     CTRL            ; 2 STOP BITS, 16*CLK,
0027  3E27                  MVI     A,27H           ; Give command.
0029  D331                  OUT     CTRL            ; CMD: RTS,ER,RXF,DTR,TXEN
002B  CD2E00                CALL    INJNK           ; Read junk twice
002E  DB30          INJNK   IN      DATA
0030  C9                    RET
0031                ;
0031                        END
SYMBOL TABLE

BAUD  0038 00  BDRT  007F 00  CINA  0000 01  COUTA 000B 01  CTRL  0031 00  DATA  0030 00
```

3.10.8 SIO in Synchronous Mode

A. Synchronous Modem Configuration

As shipped, the SIO is configured for operation as an asynchronous modem. It can be reconfigured for synchronous operation as described below.

1. Wire an 8-pin header as shown in Figure 3-12, and install it in the Clock Header socket, board location 1A.

Synchronous Modem Clock Header

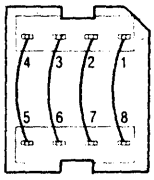


Figure 3-12

2. Remove the Configuration Header, board location 3A, and replace it with a 16-pin header wired as shown in Figure 3-13.

Synchronous Modem Configuration Header

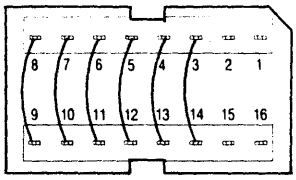


Figure 3-13

B. Synchronous Terminal Configuration

As shipped, the SIO is configured for operation as an asynchronous modem. It can be reconfigured as a synchronous terminal as described below.

1. Wire an 8-pin header as shown in Figure 3-14, and install it in the Clock Header socket, board location 1A.

Synchronous Terminal Clock Header

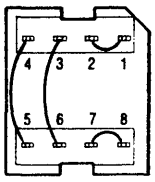


Figure 3-14

2. Remove the Configuration Header, board location 3A, and replace it with a 16-pin header wired as shown in Figure 3-15.

Synchronous Terminal Configuration Header

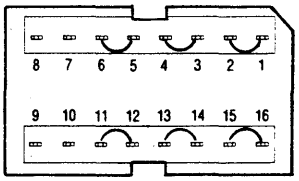


Figure 3-15

C. Synchronous Baud Rates

During synchronous operation, the receiving port speed is determined by the clock signal generated by the transmitting port. Thus, the SIO baud rate selection determines only the transmission speed for a particular port, not the receiving baud rate.

The baud rate is programmed by outputting a value to the Baud Rate register. This register is loaded via I/O address x8H, where x is determined by the board slot occupied by the SIO Board (see Table 3-22). Table 3-27 shows the values that produce the commonly used baud rates. The lowest rate is 2400 baud and the highest rate is 51K baud. Rates higher than 51K baud should not be used as this exceeds the upper frequency limit of the 8251 USART.

Table 3-27

Synchronous Baud Rate Selection		
	Baud Rate Register	
Baud Rate	Decimal	Hexadecimal
51000	122	7A
38400	120	78
19200	112	70
9600	96	60
4800	64	40
2400	0	00

D. Synchronous Programming Example

Table 3-28 provides an example of programming the SIO to communicate with a synchronous device.

Table 3-28

Sample Synchronous I/O Routines for SIO Board

```
0000                    ;
0000                    ;
0000                    ;
0000                    ;
0000                    ;     INIT initializes the USART for synchronous operation.
0000                    ;
0000                    ;     SYNI loads a received message into RAM starting
0000                    ;          at the address given in HL.
0000                    ;
0000                    ;     SYNO transmits a message from RAM starting at the
0000                    ;          address given in HL.  The number of bytes of
0000                    ;          the message is given in BC.
0000                    ;
0000                    ; As the data transferred is binary and may contain any character,
0000                    ; an escape character must be used to indicate the presence of
0000                    ; control characters such as End-of-text, Start-of-text  and Sync.
0000                    ; The escape character used is DLE, 10H.  If a DLE character
0000                    ; occurs in the data this is replaced by two DLEs in sequence.
0000                    ;
0000                    ;
0002                    STX     EQU     2       ; Start of text character
0003                    ETX     EQU     3       ; End of text character
0010                    DLE     EQU     10H     ; Data Link Escape character
0016                    SYN     EQU     16H     ; Sync character
0000                    ;
0001                    TXRDY   EQU     1       ; USART status bits
0002                    RXRDY   EQU     2
0000                    ;
0030                    PORTA   EQU     30H     ; Set for SIO boardlet in slot three.
0038                    BAUD    EQU     PORTA+8 ; Set Baud rate for channel
0030                    DATA    EQU     PORTA   ; USART data address
0031                    CTRL    EQU     PORTA+1 ; USART control/status.
0000                    ;
0078                    BDRT    EQU     120     ; Set Baud rate of 38.4 Khz
0000                    ;
0000  3E78              INIT    MVI     A,BDRT  ; Set Baud rate
0002  D338                      OUT     BAUD    ; for SIO boardlet
0004  3E80                      MVI     A,80H   ; Ensure USART is cleared
0006  D331                      OUT     CTRL    ; as specified by manufacturers
0008  D331                      OUT     CTRL
000A  3E40                      MVI     A,40H   ; do reset
000C  D331                      OUT     CTRL
000E                    ;
000E  3E0C                      MVI     A,0CH   ; Double sync, no parity
0010  D331                      OUT     CTRL
0012  3E10                      MVI     A,DLE   ; Sync character #1
0014  D331                      OUT     CTRL
0016  3E16                      MVI     A,SYN   ; Sync character #2
0018  D331                      OUT     CTRL
001A  3EB7                      MVI     A,0B7H  ; Hunt,RTS,Error reset,RxE,DTR,TxE
001C  D331                      OUT     CTRL
001E  DB30                      IN      DATA    ; Read junk
0020  C9                        RET
0021                    ;
0021                    ; Synchronous input routine (RAM address in HL)
0021                    ;
0021  CD0000            SYNI    CALL    INIT    ; Set USART into hunt mode and
0024  CD5100                    CALL    GETCH   ; reset errors
```

Table 3-28 (continued)

```
0027  FE10            CPI   DLE
0029  20F6            JRNZ  SYNI    ; Wait for DLE to appear
002B  CD5100          CALL  GETCH
002E  FE16            CPI   SYN     ; If SYNC, try again
0030  28EF            JRZ   SYNI
0032  FE02            CPI   STX     ; Check for start of text,
0034  20EB            JRNZ  SYNI    ; if bad, try again
0036            ;
0036            ; Transfer message into RAM
0036            ;
0036  CD5100    SDATA CALL  GETCH
0039  FE10            CPI   DLE
003B  2010            JRNZ  RAMLD   ; If not DLE then data
003D  CD5100          CALL  GETCH   ; Get second char of DLE seq
0040  FE10            CPI   DLE     ; If DLE-DLE then use one
0042  2809            JRZ   RAMLD   ; of them as data
0044  FE16            CPI   SYN     ; Check for padding (SYNC chars)
0046  28EE            JRZ   SDATA   ; ignore if it is
0048  FE03            CPI   ETX     ; End yet ?
004A  C8              RZ    ;       ; If not done, then bad DLE
004B  18E9            JR    SDATA   ; sequence found, ignore it
004D            ;
004D  77        RAMLD MOV   M,A     ; Insert byte into RAM at (HL)
004E  23              INX   H
004F  18E5            JR    SDATA   ; Get next byte
0051            ;
0051  DB31      GETCH IN    CTRL    ; Get char from serial port
0053  E602            ANI   RXRDY
0055  28FA            JRZ   GETCH   ; Wait till done
0057  DB30            IN    DATA
0059  C9              RET
005A            ;
005A            ; Synchronous output routine
005A            ; Outputs BC characters starting at address in HL
005A            ;
005A  CD0000    SYNO  CALL  INIT    ; Reset USART
005D  C5              PUSH  B       ; Save byte count
005E  0600            MVI   B,0     ; Send 255 DLE-SYNCs
0060  3E10      HEADR MVI   A,DLE   ; before message
0062  CD9100          CALL  OPCH
0065  3E16            MVI   A,SYN
0067  CD9100          CALL  OPCH
006A  10F4            DJNZ  HEADR
006C  C1              POP   B       ; Restore byte count
006D            ;
006D  3E10            MVI   A,DLE   ; Send message header of
006F  CD9100          CALL  OPCH    ; DLE STX
0072  3E02            MVI   A,STX
0074  CD9100          CALL  OPCH
0077            ;
0077            ; Transfer message contents
0077            ;
0077  7E        NCHO  MOV   A,M
0078  CD9100          CALL  OPCH    ; Output byte of data
007B  3E10            MVI   A,DLE   ; DLE for comparison
007D  EDA1            CPII  ;       ; Check if char was DLE and count
007F  CC9100          CZ    OPCH    ; Output second DLE if it was
0082  EA7700          JPE   NCHO    ; Loop till done
0085  CD9100          CALL  OPCH    ; Output DLE from A
```

Table 3-28 (continued)

```
0088  3E03              MVI    A,ETX   ; Send End of text
008A  CD9100            CALL   OPCH    ;
008D  CD0000            CALL   INIT    ; Stop SYNC characters
0090  C9                RET    ;       ; Return to calling program
0091                ;
0091  F5          OPCH  PUSH   PSW     ; Output Character
0092  DB31        WTX   IN     CTRL    ; Get USART status
0094  E601              ANI    TXRDY   ; Check if ready for character
0096  28FA              JRZ    WTX     ; Wait till it is
0098  F1                POP    PSW     ; Get character back and
0099  D330              OUT    DATA    ; output
009B  C9                RET
009C                ;
009C                    END
SYMBOL TABLE

BAUD  0038 00  BDRT  0078 00  CTRL  0031 00  DATA  0030 00  DLE   0010 00  ETX   0003 00
```

3.11 PIO BOARD

The PIO (Parallel Input Output) Board is used to drive parallel printers and other devices requiring transfer of data in 8-bit parallel form.

The PIO Board contains a configuration header which allows it to adapt to many different device interfaces. This header changes the way that the components on the board are connectedto external devices. Since the header can be wired in many ways, only one configuration is discussed here, i.e., with the header wired as shown in Figure 3-16.

Standard PIO Configuration Header

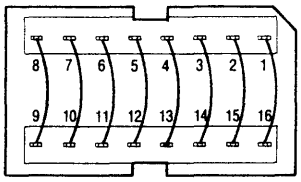


Figure 3-16

This is the standard North Star configuration. To determine the affect that other configurations would have on the operation and programming of the PIO board, refer to the PIO board schematic in Appendix I.

3.11.1 Reset

When the I/O Reset bit (I/O address F0H, bit 4) is set on, then off, its only effect on the PIO Board is to reset the Interrupt Mask to all zeros. The Interrupt Mask is described in Section 3.11.4 below. The I/O Reset bit resets all I/O boards simultaneously.

The standard 'beep' sound is a 1920 Hz tone with a duration of one-half second. This sound is produced by inputting from I/O address 83H. The input data is indeterminate.

The programmable sound is produced by manipulating bit 6 of the I/O Control register (I/O address F0H). When this bit is complemented at the proper rate, a tone is produced in the speaker. For example, complementing the bit once every millisecond will produce a 500 Hz tone. The tone is maintained as long as the bit is being complemented. Note that complex sounds may be generated by complementing the bit at an irregular rate.

3.13 BOOTSTRAP FIRMWARE

The Bootstrap program is contained in the Boot PROM (see Section 4.1.3). The Bootstrap program loads other programs from diskette or from a serial port via an SIO Board.

3.13.1 Startup

The Bootstrap program may be entered by generating a non-maskable interrupt (see Section 3.3.2), or by executing the following two instructions:

1. Output 84H to I/O address A2H.

2. Jump to address 8066H.

When the Bootstrap program is entered, it performs the following sequence:

1. The Z80 processor registers are pushed into the existing stack in the following sequence: AF,B,D,H, alternate AF, alternate B, alternate D, alternate H, alternate IX and alternate IY. Finally, the interrupt vector is pushed.

2. The stack pointer is put in register IY. If the Bootstrap program was entered as the result of a power reset, register IY contains 0001H.

3. The Display RAM is mapped into 0000H through 7FFFH, the Boot PROM is mapped into 8000H through BFFFH, and the first 16K bytes of Main RAM are mapped into C000H through FFFFH.

4. A beep sounds, and the message 'LOAD SYSTEM' is displayed.

The Bootstrap program then waits for instructions entered from the keyboard. These instructions may cause it to boot from drive 1, boot from drive 2, or boot from a serial port (see Section 2.2).

3.13.2 Boot from Disk Drive

NOTE
The ADVANTAGE HD-5 cannot be cold booted from the hard disk.

If the Bootstrap program is directed to boot from one of the floppy disk drives, it performs the following sequence:

1. Sectors 4,5,6 and 7 on track 0 are read into Main RAM. The first data byte in sector 4 determines the starting location of the area in Main RAM in which the program is stored.

   For example, if the first data byte is C0H, this byte is stored in location C000H, and remaining data bytes in sectors 4,5,6 and 7 are stored sequentially from that point. This first byte must be in the range C0H through F8H.

2. The first 16K bytes of Main RAM are mapped into 0000H through 3777H and 4000H through 7FFFH.

3. A jump is made to the load address + 10. This location must contain the op code for a jump instruction.

If the boot attempt is unsuccessful, a beep sounds and the 'LOAD SYSTEM' message is redisplayed. There are five ways that a failure may occur:

1. Diskette not loaded.

2. Machine malfunction.

3. Uncorrectable read error (wrong CRC byte). The CRC byte is calculated by the routine shown in Table 3-33.

4. Wrong sync byte. The first sync byte is FBH. The second sync byte is the sector number plus 16 times the track number, truncated to eight bits.

5. The first byte of sector 4 is not in the range C0H through F8H, or the tenth byte of sector 4 is not C3H.

Table 3-33

Boot PROM CRC Routine

```
814E   DB80      READL  IN     RDATA  ;GET BYTE
8150   FEC0             CPI    0C0H
8152   D8               RC
8153   FEF9             CPI    0F9H
8155   D0               RNC
8156   57               MOV    D,A ; MSB OF STORE ADDRESS
8157   12               STAX   D ;STORE IT ALSO
8158   13               INX    D
8159   07               RLC
815A   4F               MOV    C,A ;START OF CRC VALUE
815B   216581           LXI    H,BLOOP ;SET NEW RETURN ADDRESS
815E   DB80             IN     RDATA ;GET SECOND BYTE
8160   12               STAX   D
8161   13               INX    D
8162   A9               XRA    C
8163   07               RLC    ;CRC CALC
8164   4F               MOV    C,A
8165   DB80      BLOOP  IN     RDATA ;READ DATA LOOP
8167   12               STAX   D
8168   A9               XRA    C ;FORM CRC
8169   07               RLC
816A   4F               MOV    C,A
816B   13               INX    D ;UPDATE STORE ADDRESS
816C   DB80             IN     RDATA ;SECOND BYTE
816E   12               STAX   D
816F   A9               XRA    C
8170   07               RLC
8171   4F               MOV    C,A
8172   13               INX    D
8173   10F0             DJNZ   BLOOP
8175            ;HAVE COMPLETED A BLOC, GET CRC
8175   DB80             IN     RDATA ;CRC BYTE
8177   A9               XRA    C ;SEE IF IT MATCHES COMPUTED CRC
8178   DB82             IN     RENBL ;CLEAR READ ENABLE
817A   20A1             JRNZ   READA ;IF NOT, GO READ AGAIN
```

3.13.3 Boot from Serial Port

In order to use this feature, an SIO board must be installed in I/O slot 3, and the board ID must be in the range F0H through F7H. The board must be configured for synchronous operation and connected to a synchronous communication link.

If the Bootstrap program is directed to boot from serial port, it configures the USART as follows:

Synchronous Mode
2400 baud
Two sync bytes - DLE,SYN
Eight bits per word
Two stop bits
Parity off

After the USART is configured, it should be receiving sync bytes. If sync is not detected within 1 second, a beep sounds and 'LOAD SYSTEM' is redisplayed. If sync is detected, the following 'dialogue' should occur:

```
Other system:DLE,SYN,ENQ,PAD          "WHAT DO YOU WANT?
ADVANTAGE:DLE,SYN,EOT,NUM,ENQ PAD "I WANT THE PROGRAM"
Other system:STX,<data>,ETX,SUMLO,       "HERE IT IS"
                          SUMHI, PAD
```

STX=02H,ETX=03H,EOT=04H,ENQ=05H,DLE=10H,SYN=16H,PAD=0FFH
NUM = boot type number (01H for the ADVANTAGE)
SUMHI,SUMLO=checksum computed as((sum of all data bytes) +1) mod 65536

The Boot program can wait indefinitely for the "What do you want?" message. When it is received, it sends the "I want the program" message. Then it can wait indefinitely for the STX. When the STX arrives, the Boot program assumes that subsequent data is the program.

The first byte after the STX determines the starting location of the area in Main RAM into which the program is loaded. For example, if the first byte is C0H this byte is stored in location C000H, and the remainder of the program is stored sequentially from that point. This first byte must be in the range C0H through F8H.

The DLE character has special significance in the data stream as follows:

1. Two DLE's in a row are stored as one DLE.

2. Pairs of sync bytes DLE, SYN are dropped.

3. DLE,DLE,SYN is stored as DLE,SYN.

4. Single DLEs not followed by SYN or ETX are dropped.

5. The pair DLE,ETX signals end of program and is not stored.

Only those bytes that are stored in the RAM are included in the checksum. The checksum is computed as ((sum of all data bytes)+1) mod 65536. If the computed checksum does not match the checksum in the message, a beep sounds and the message 'LOAD SYSTEM' is redisplayed. If the checksums match, the first 16K bytes of Main RAM is mapped into locations 0000H through 3FFFH and 4000H through 7FFFH, and a jump is made to the load address + 10.

The ADVANTAGE System Block Diagram

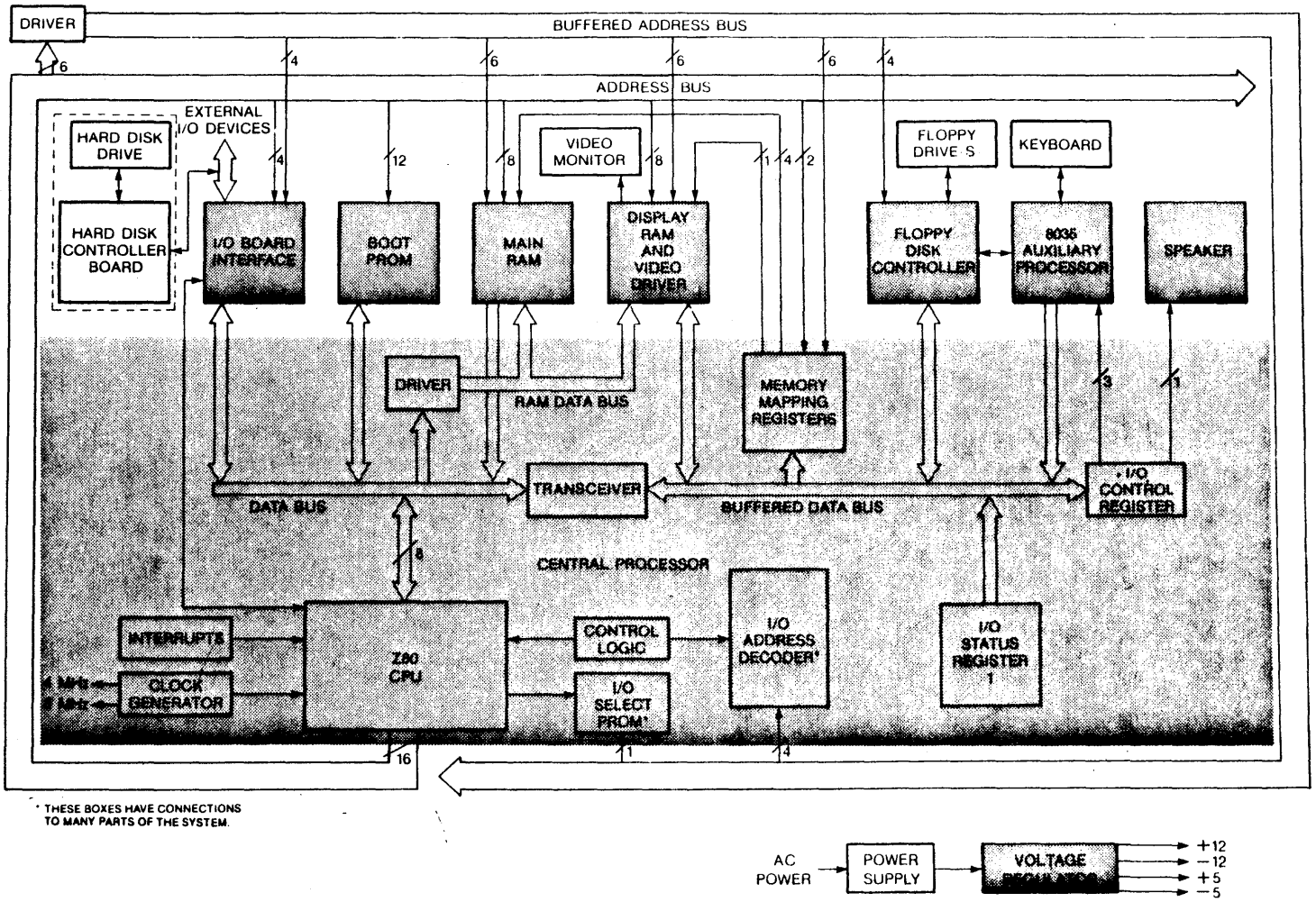


Figure 4-1

Central Processor Block Diagram

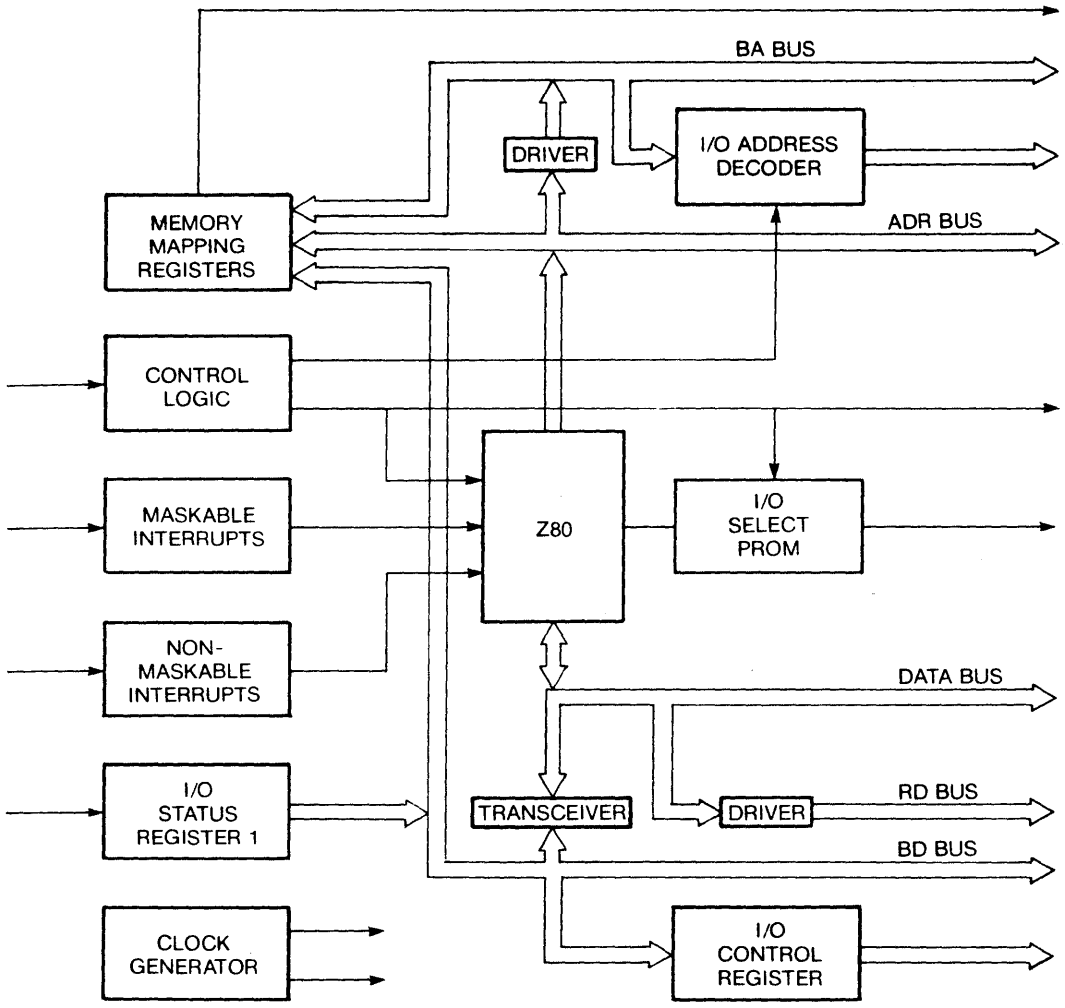


Figure 4-2

4.1.5 Floppy Disk Controller

The Floppy Disk Controller performs most of the control functions for the disk drives. It selects the drive, selects a side on the diskette, positions the read/write head and performs the read or write operation.

The Auxiliary Processor performs the remaining floppy disk operations, controlling of the disk motors and keeping track of the sector number.

A block diagram of the Floppy Disk Controller is shown in Figure 4-6.

The Data Separation Circuitry receives a signal from the selected disk drive which contains both data and clocks. It synchronizes with the clocks, removes the clocks from the signal, and sends the data in serial form to the Control Logic. Three major signals control the Data Separation Circuitry: DISK READ FLAG, ACQUIRE and BUFACQUIRE. The DISK READ FLAG enables the Data Separation Circuitry. The ACQUIRE and BUFACQUIRE signals are set only during the preamble of the sector when there are clock pulses but no data pulses. They allow the phase lock loop in the Data Separation circuitry to quickly synchronize with the clock.

Disk Controller Block Diagram

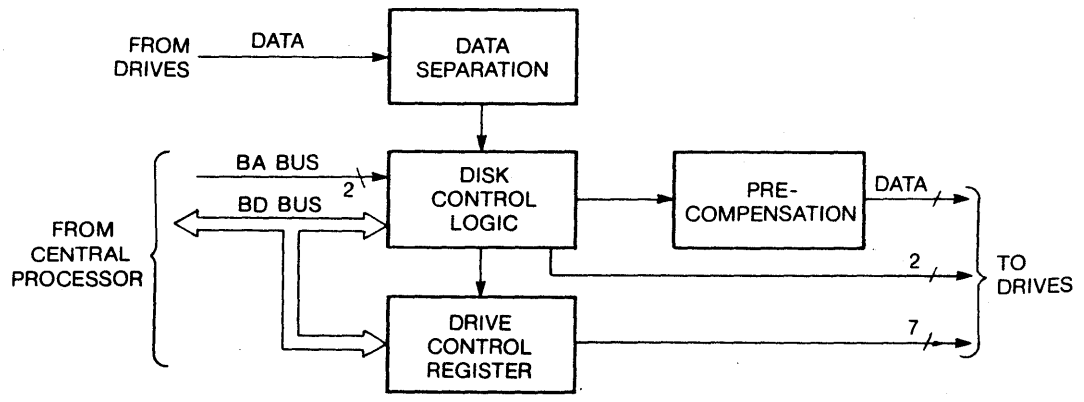


Figure 4-6

The Control Logic responds to the eight I/O instructions listed in Table 4-7. The Control Logic detects these instructions by comparing bits 0 and 1 of the BA bus, and signals $\overline{WR}$, $\overline{RD}$ and $\overline{DISK\ I/O}$ from the Central Processor. 8-bit bytes are transferred between the Control Logic and the Central Processor via the BD bus.

Table 4-7

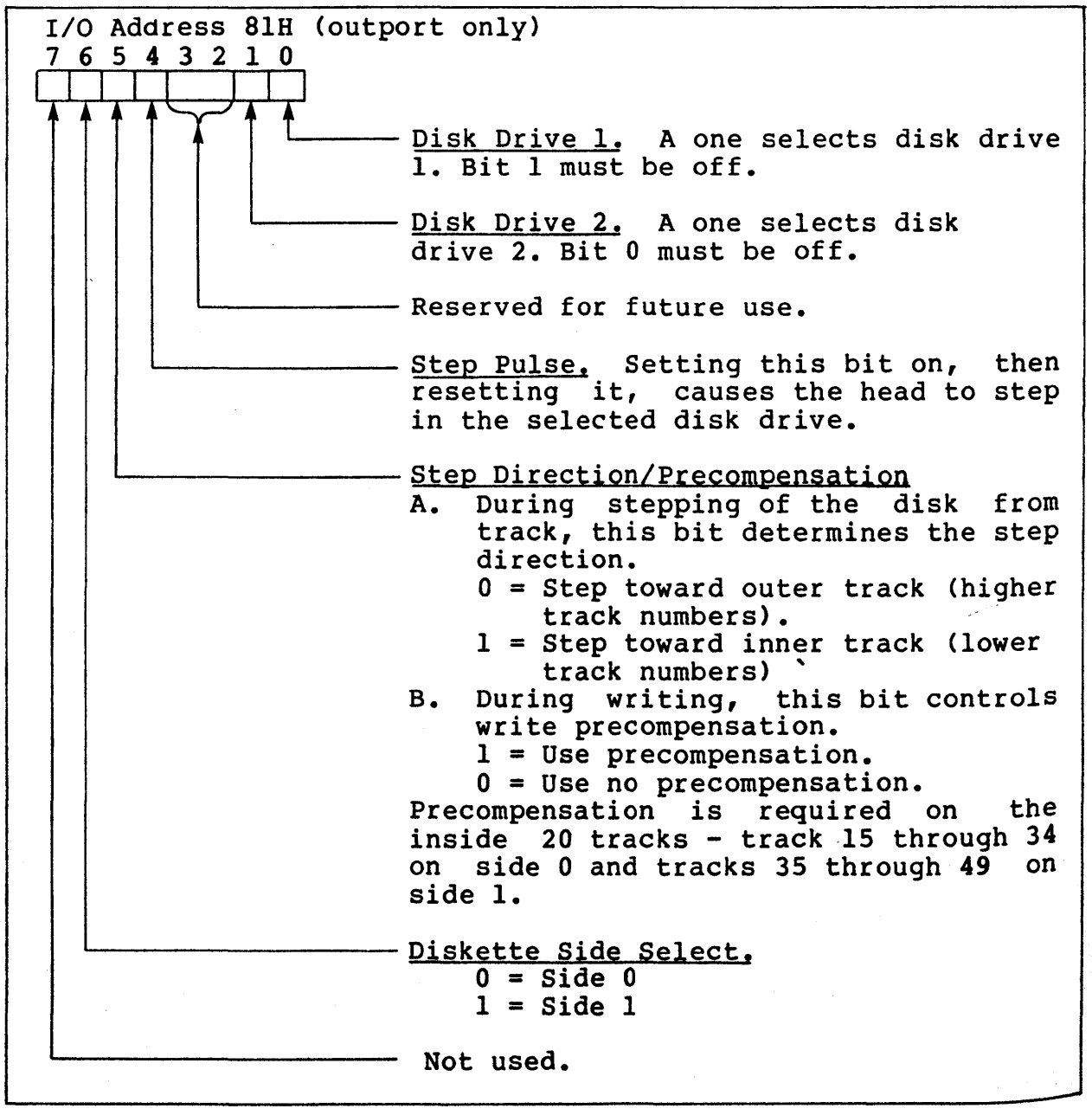
Floppy Disk I/O Instructions

I/O Address (Hexadecimal)	Operation	Description
80	INPUT	Input disk data.
80	OUTPUT	Output disk data.
81	INPUT	Input sync byte.
81	OUTPUT	Load drive control register.
82	INPUT	Clear Disk Read flag.
82	OUTPUT	Set Disk Read Flag.
83	INPUT	Produce the standard 'beep' sound. The decoded signal is sent to the Speaker Circuit (see Figure 4-1).
83	OUTPUT	Set Disk Write flag.

The Floppy Disk Drive Control Register stores a control byte which comes from the Central Processor and is sent directly to the disk drives. Table 4-8 shows the format of the register.

Table 4-8

Floppy Disk Drive Control Register Format



The Precompensation circuit changes the timing of the data and clock pulses that are written on the inside tracks of the diskette. The pulse timing must be changed because of the higher density of the data on these tracks.

4.1.6 Display RAM and Video Generator

The Display RAM has a storage capacity of 20K bytes, with 8 bits per byte. This RAM stores the data displayed on the ADVANTAGE video monitor. Section 3.6.1 explains the correlation between the bits in memory and the dots (pixels) on the screen.

The Video Generator serializes the data in the Display RAM and sends this data to the Video Monitor, along with horizontal and vertical sync pulses. It also allows the Central Processor to gain access to the Display RAM, and implements vertical scrolling of the displayed data.

Figure 4-7 shows a block diagram of the Display RAM and Video Generator. All blocks in the diagram are part of the Video Generator except the one marked 'RAM'.

When the Central Processor writes data into the Display RAM, the Address Mux (multiplexer) directs address bits from the BA and ADR buses to the RAM. The data to be written enters the RAM from RD bus.

When the Central Processor reads data from the RAM, the Address MUX again directs the address bits from the BA and ADR buses to the RAM, but the data from the RAM is placed on the BD bus.

The RAM is automatically refreshed as a result of reading video data during generation of the video signal.

4.1.7 I/O Board Interface

The I/O Board Interface consists of six PC board connectors and associated bus drivers and decoders. The I/O boards inserted in these connectors respond to I/O instructions from the Central Processor. The boards may communicate only with the Central Processor, or they may interface the Central Processor to an external device.

Figure 4-10 is a block diagram of the I/O Board Interface.

I/O Board Interface Block Diagram

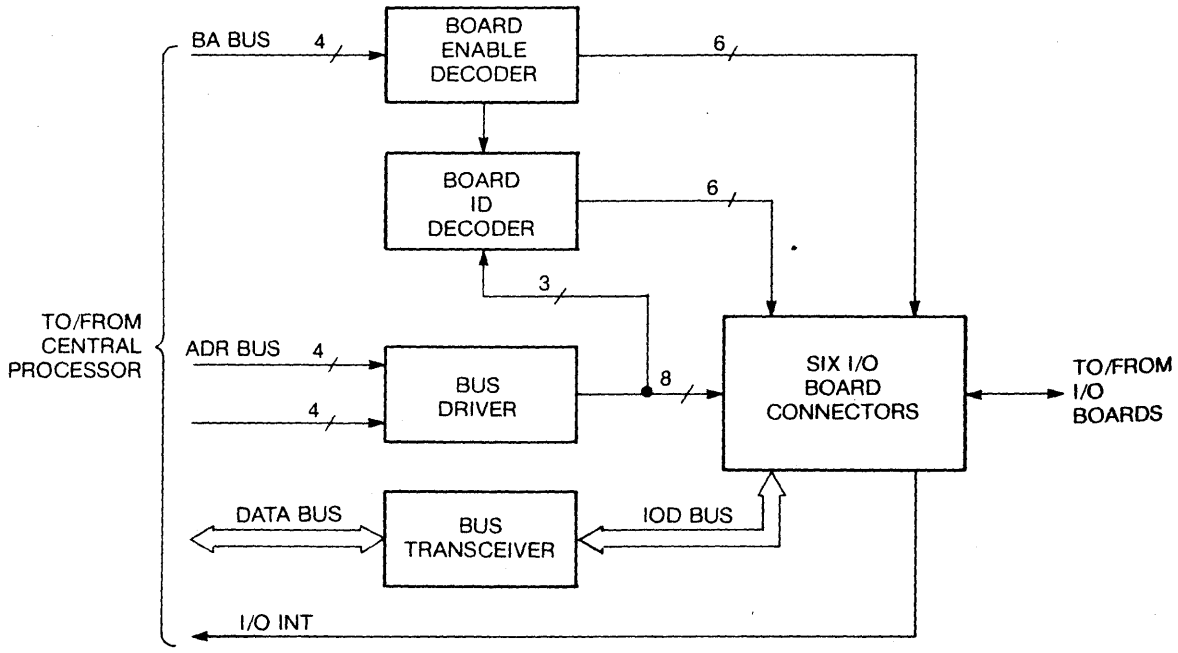


Figure 4-10

The Board Enable Decoder decodes the upper four bits of the I/O address, taken from the BA bus. It provides each of the board connectors with an enable signal (ENA I/O 1 through ENA I/O 6). Each board must complete the decoding of the I/O address and the recognition of I/O instructions by comparing signals sent to it from the Bus Driver.

The Board ID Decoder responds to I/O instructions with an I/O address of 70 through 75 and 78 through 7D. These instructions input the identification code of the board in a particular board connector. The decoder provides one ID REQ signal for each connector. The ID code returns to the Central Processor via the IOD and DATA buses.

The Bus Driver continually transfers the lower four bits of the address bus and four control and timings signals from the Central Processor to all board connectors. The I/O boards use these signals, in conjunction with those sent from the Board Enable Decoder and the Board ID Decoder to complete the recognition of specific I/O instructions.

The Bus transceiver transfers 8-bit bytes of data between the Central Processor and the I/O Boards. The Central Processor controls the direction of data flow.

The I/O Boards use the $\overline{\text{I/O INT}}$ signal to send interrupt requests to the Central Processor.

The signals on the six I/O Board connectors are defined in Table 4-13. All signals are common to all connectors, except the signals on pin 3 and pin 29. These are the individual 'board select' signals from the Board Enable Decoder and the Board ID Decoder.

Table 4-13

I/O Board Pin Assignments

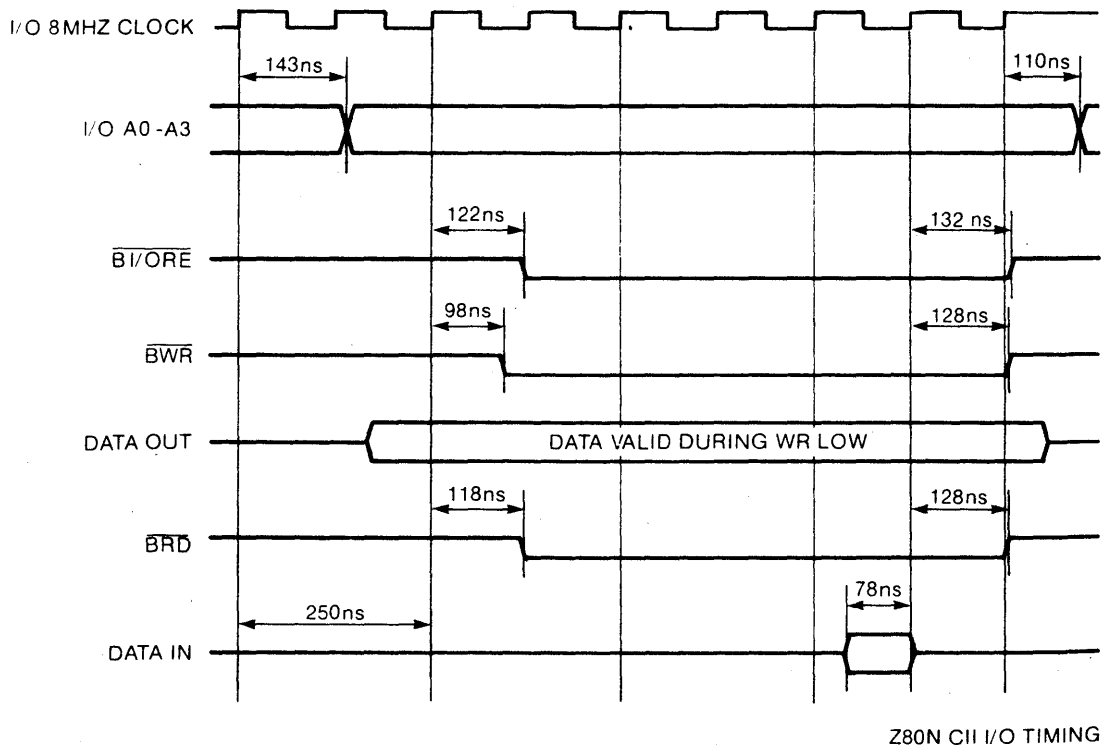
Pin	Signal Name	Signal Direction	Function
1	Ground		Power/signal ground
2			Not used.
3	$\overline{\text{ID REQ}}$	OUTPUT	Input board identification code
4	+5V	OUTPUT	DC power
5	+12V	OUTPUT	DC power
6			Not used
7	$\overline{\text{IO INT}}$	INPUT	Maskable interrupt request
8			Not used
9	IOA2	OUTPUT	Buffered Address bus, bit 2
10	IOA1	OUTPUT	Buffered Address bus, bit 3
11	IOA1	OUTPUT	Buffered Address bus, bit 1
12	Ground		Power/signal ground
13	$\overline{\text{BRD}}$	OUTPUT	Buffered Z80 processor $\overline{\text{RD}}$ signal
14	IOA0	OUTPUT	Buffered Address bus, bit 0
15	IO8MHz	OUTPUT	8 MHz clock
16	$\overline{\text{BWR}}$	OUTPUT	Buffered Z80 processor $\overline{\text{WR}}$ signal
17	IOD3	BIDIRECTIONAL	I/O Data bus, bit 3
18	$\overline{\text{BIORES}}$	OUTPUT	Resets I/O boards
19	IOD2	BIDIRECTIONAL	I/O Data bus, bit 2
20	IOD4	BIDIRECTIONAL	I/O Data bus, bit 4

Table 4-13 (continued)

Pin	Signal Name	Signal Direction	Function
21	Ground		Power/signal ground
22	I0D5	BIDIREC-TIONAL	I/O Data bus, bit 5
23	I0D6	BIDIREC-TIONAL	I/O Data bus, bit 6
24	I0D1	BIDIREC-TIONAL	I/O Data bus, bit 1
25	I0D0	BIDIREC-TIONAL	I/O Data bus, bit 0
26	-12V	OUTPUT	DC power
27	+5V	OUTPUT	DC power
28	I0D7	BIDIREC-TIONAL	I/O Data bus, bit 7
29	$\overline{\text{ENA I/O}}$	OUTPUT	Selects board for I/O operation
30	Ground		Power/signal ground

Figure 4-11 shows the timing of the I/O Board signals. Both read and write cases are shown, although the WR and DATA OUT signals would only be active during an output instruction and the RD and DATA IN signals would only be active during an input instruction.

I/O Board Timing



WAVEFORMS DRAWN FOR WORST CASE.

Figure 4-11

4.3 SIO BOARD

The SIO (Serial Input/Output) Board interfaces the Main PC Board with serial printers and communication links. The board's serial interface can be configured to support the RS232 standard or current loop operation. A block diagram of the SIO Board is shown in Figure 4-14.

The SIO Board supports either synchronous or asynchronous operation. It is initially configured as an asynchronous modem. Pin assignments for asynchronous operation are shown in Figure 4-15. Pin assignments for synchronous operation are shown in Figure 4-16.

The heart of the SIO board is the 8251 USART. Refer to the manufacturer's data sheet in Appendix H for information concerning this integrated circuit.

SIO Board Block Diagram

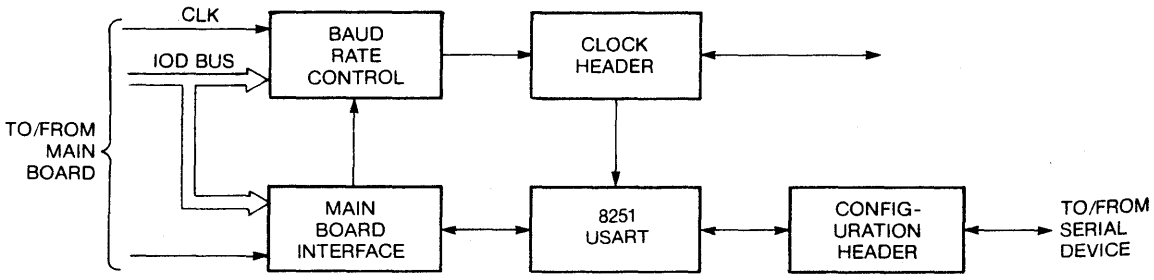


Figure 4-14

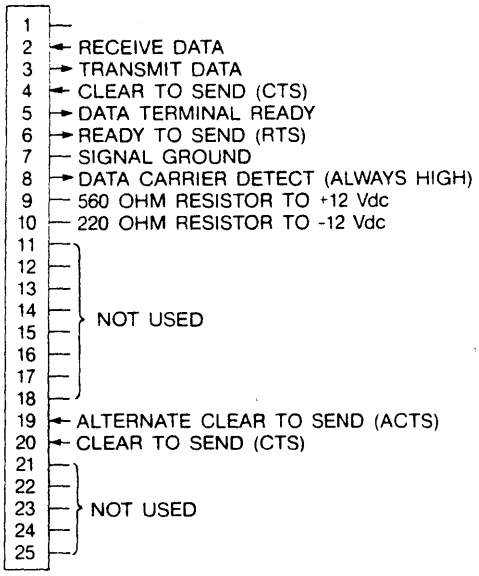
The Main Board Interface responds to I/O instructions from the Main PC Board. All but one of these instruction are listed in Table 4-15. The unlisted instruction is directed to the I/O board connector rather than the SIO board. It requests that the board in that connector place its board ID code on the IOD bus. When this instruction is active, the ID REQ signal goes low. The ID code for the SIO Board is F7H.

The Interrupt Mask is a 4-bit register contained in the Main Board Interface. It determines the conditions under which a maskable interrupt is sent to the Main PC Board. Each bit of the register is associated with an output bit of the USART. When the mask bit is a one and the associated USART signal is true, the interrupt is generated. Figure 4-16 shows the format of the register.

The Clock Header is an 8-pin jumper plug which mates with an 8-pin IC (see Figure 3-12) socket on the SIO board. This header is used only for synchronous operation. It allows the receive and transmit clocks to be rerouted so the receive clock originates from the serial device (connector J1) and the transmit clock is supplied to that device.

The Configuration Header is a 16-pin jumper plug which mates with a 16-pin IC socket on the SIO board. This header allows the interface signals between the USART and the serial device to be wired so as to conform to the requirements of the device.

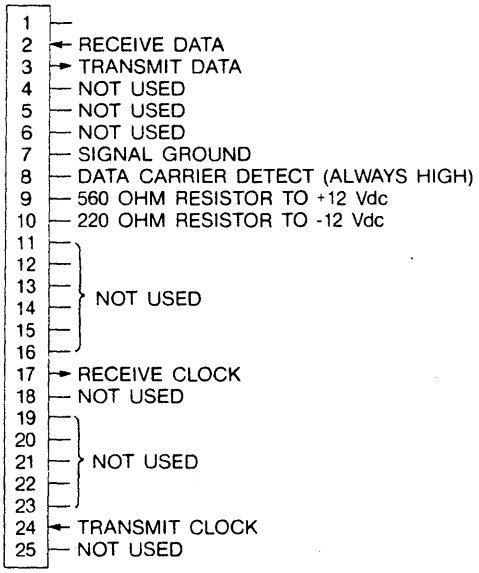
SIO Connector Pin Assignments (Asynchronous)



NOTES:
1. Connector view from ADVANTAGE SIO
2. Connect cable shield to Pin 1 and connector retaining screws. This connection provides an adequate protective connection to the ADVANTAGE chassis ground.
3. For other asynchronous requirements, see SIO board Schematic.

Figure 4-15

SIO Connector Pin Assignments (Synchronous)



NOTES:
1. Connector view from ADVANTAGE SIO
2. Connect cable shield to Pin 1 and connector retaining screws. This connection provides an adequate protective connection to the ADVANTAGE chassis ground.
3. For other synchronous requirements, see SIO board Schematic.

Figure 4-16

Table 4-15

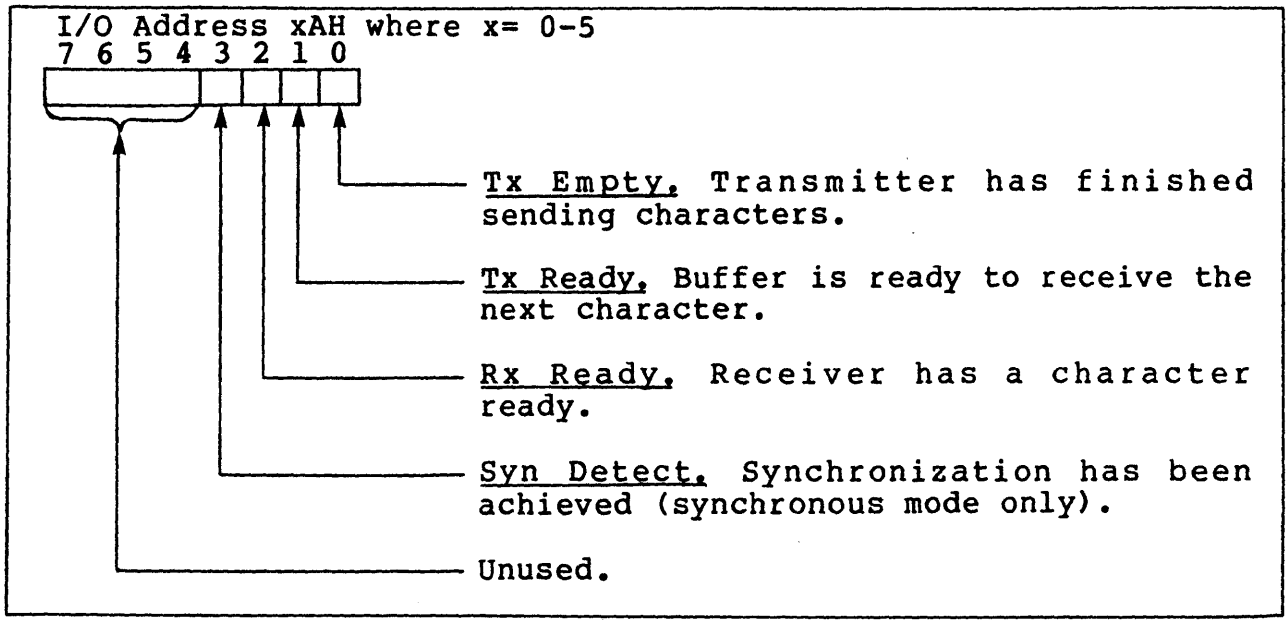
SIO Board I/O Instructions

I/O Address (Hexadecimal)	Operation	Description
X0	INPUT	Transfer a data byte from the USART to the Main PC Board.
X0	OUTPUT	Transfer a data byte from the Main PC Board to the USART.
X1	INPUT	Transfer a status byte from the USART to the Main PC Board.
X1	OUTPUT	Transfer a control byte from the Main PC Board to the USART.
X8 or X9	OUTPUT	Load the Baud Rate register.
XA or XB	OUTPUT	Load the Interrupt Mask register.

NOTE: The first digit of these I/O addresses selects one of the six I/O board connectors. If the connector is enabled, signal $\overline{\text{ENA IO}}$ is low.

Table 4-16

SIO Interrupt Mask Format



The Baud Rate Control section provides two clocks for the USART: the USART clock and the baud clock.

The USART clock is the fixed frequency basic clock signal for the USART. It is produced by dividing the Main PC Board 8MHz clock signal by 4.33.

The baud clock is used by the USART to determine its transmitting and receiving frequency. The baud clock is generated by a combination of the Baud Rate register and a 7-bit counter. The Baud Rate register provides the pre-load value for the low order 8 bits of the counter. The counter clock is developed by dividing the Main PC Board 8MHz clock signal by 13. The USART provides the frequency:

$$\frac{8\text{MHz}}{13 \times 2 \times (128 - \text{Baud Rate Register})}$$

6.2.5 SIO Board Test

The SIO Test Diagnostic checks for the presence of an SIO Board and performs rudimentary testing. Before running this diagnostic, connect a special test plug to the RS-232 connector of the SIO Board. This connector is located on the rear panel of the ADVANTAGE. The test plug can be made with a male RS-232 connector as follows:

Connect: pin 2 to pin 3 (RxD to TxD)
pin 4 to pin 5 (DSR to DTR)
pin 8 to pin 20 (CTS low)

A sample display is shown in Figure 6-6, indicating one SIO Board in connector J5.

SIO Board Test - Display Format

```
NO SIO BOARD IN SLOT 6
TESTING SIO BOARD IN SLOT 5
  BOARD PASSED AT 9600 BAUD
NO SIO BOARD IN SLOT 4
NO SIO BOARD IN SLOT 3
NO SIO BOARD IN SLOT 2
NO SIO BOARD IN SLOT 1
I'm done now!

Type any character to continue.
```

Figure 6-6.

7.2 TROUBLESHOOTING PROCEDURES

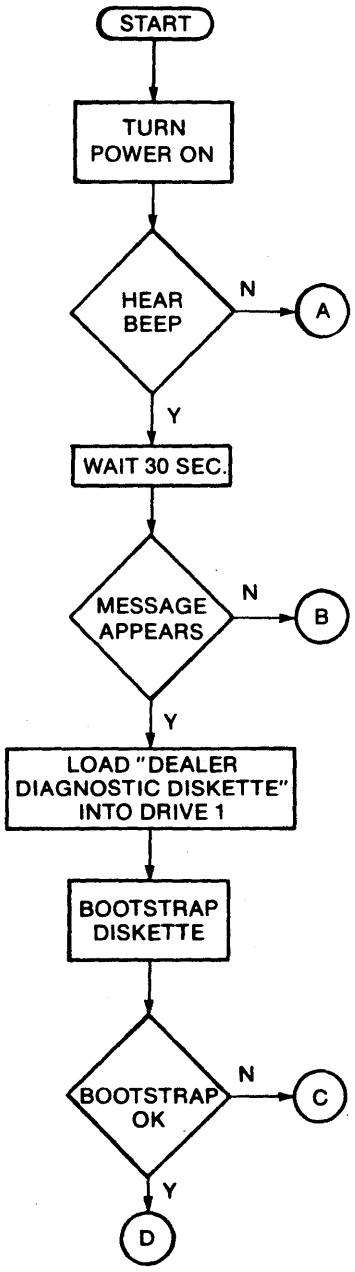
Run the Mini Monitor general diagnostic and the dedicated diagnostics, and use the troubleshooting chart (Figure 7-1) to help isolate the fault to a subassembly that can be replaced.

7.2.1 Troubleshooting Chart

The troubleshooting chart is a typical flow chart with process and decision blocks. Rectangular blocks indicate a manual process and decision blocks question whether a particular operational process has occurred.

NOTE
ALWAYS check power supply voltages FIRST.

ADVANTAGE Troubleshooting Chart



COMMENTS

Message consists of the words "LOAD SYSTEM" accompanied by a cursor. The rest of the screen is blank.

Instructions for loading diskettes and bootstrapping are in Section 2.2.

Bootstrap is successful if screen message changes to "Integrity Test".

Figure 7-1

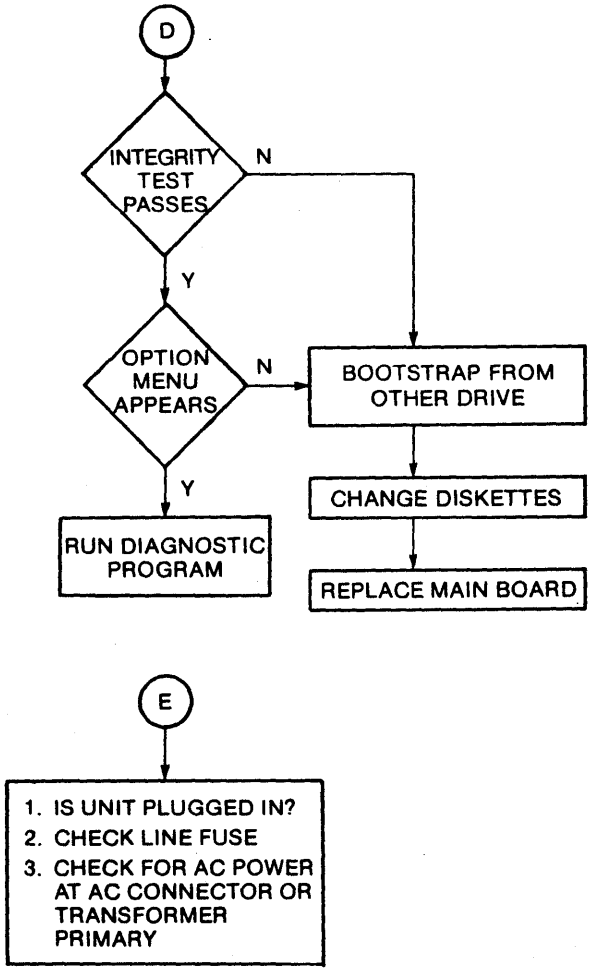
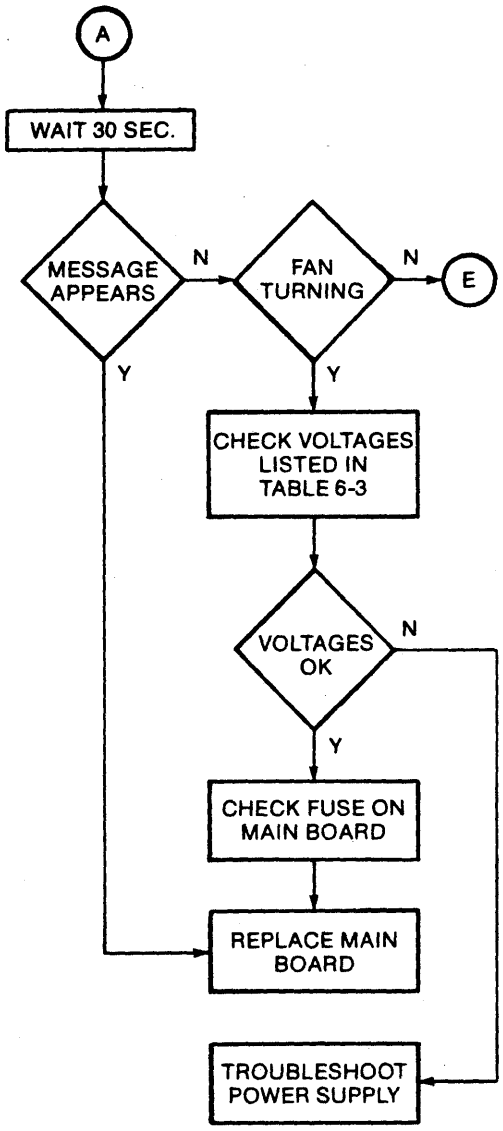


Figure 7-1 (continued)



COMMENTS

Message consists of the words "LOAD SYSTEM" accompanied by a cursor. The rest of the screen is blank.

Fuse is located in right rear corner of board.

See Appendix F, Main PCB Schematic.

Figure 7-1 (continued)

Figure 7-1 (Continued)

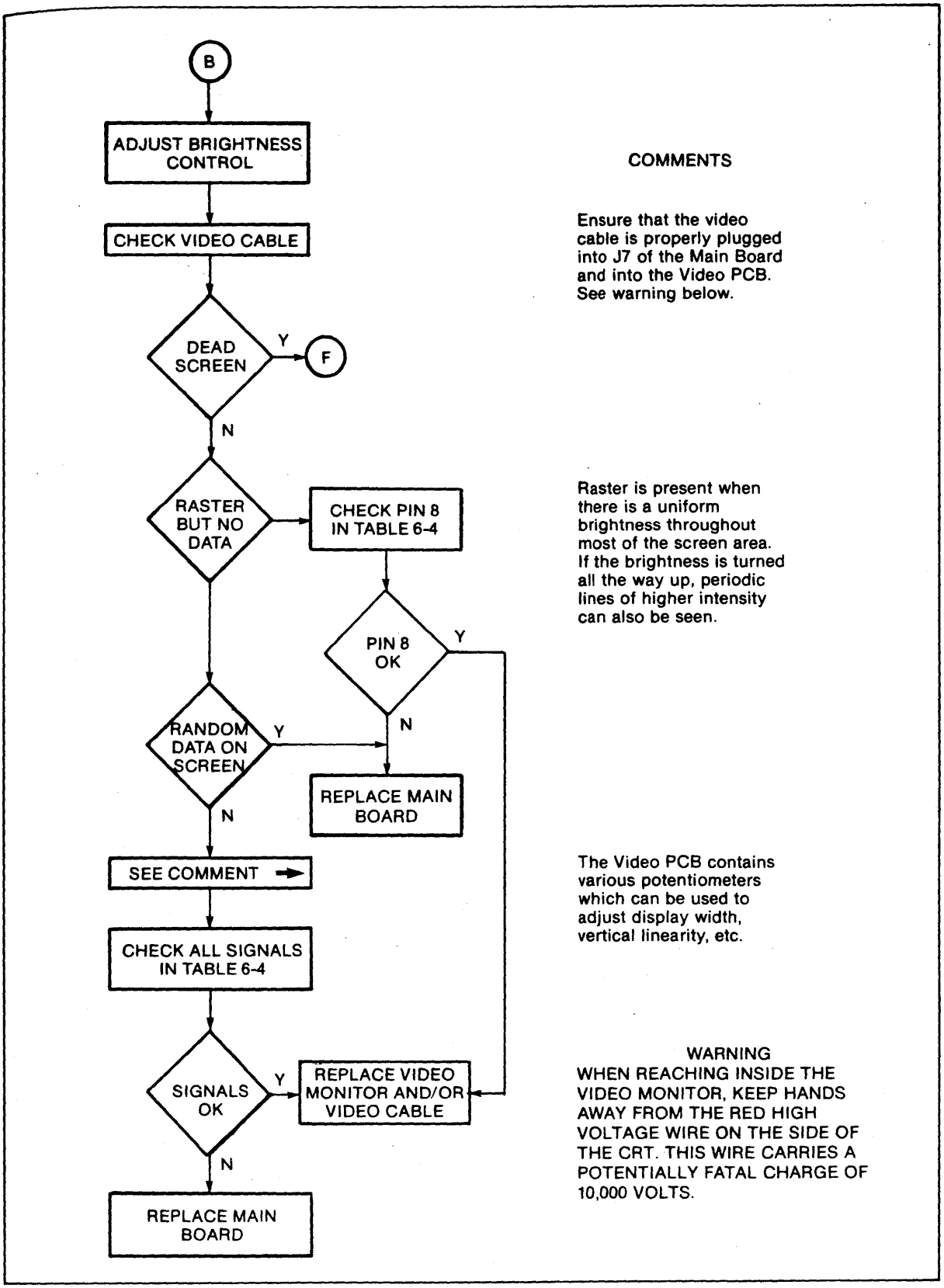
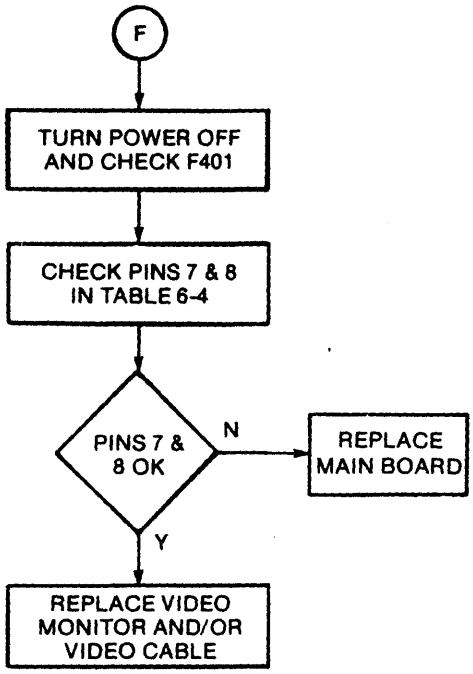


Figure 7-1 (Continued)

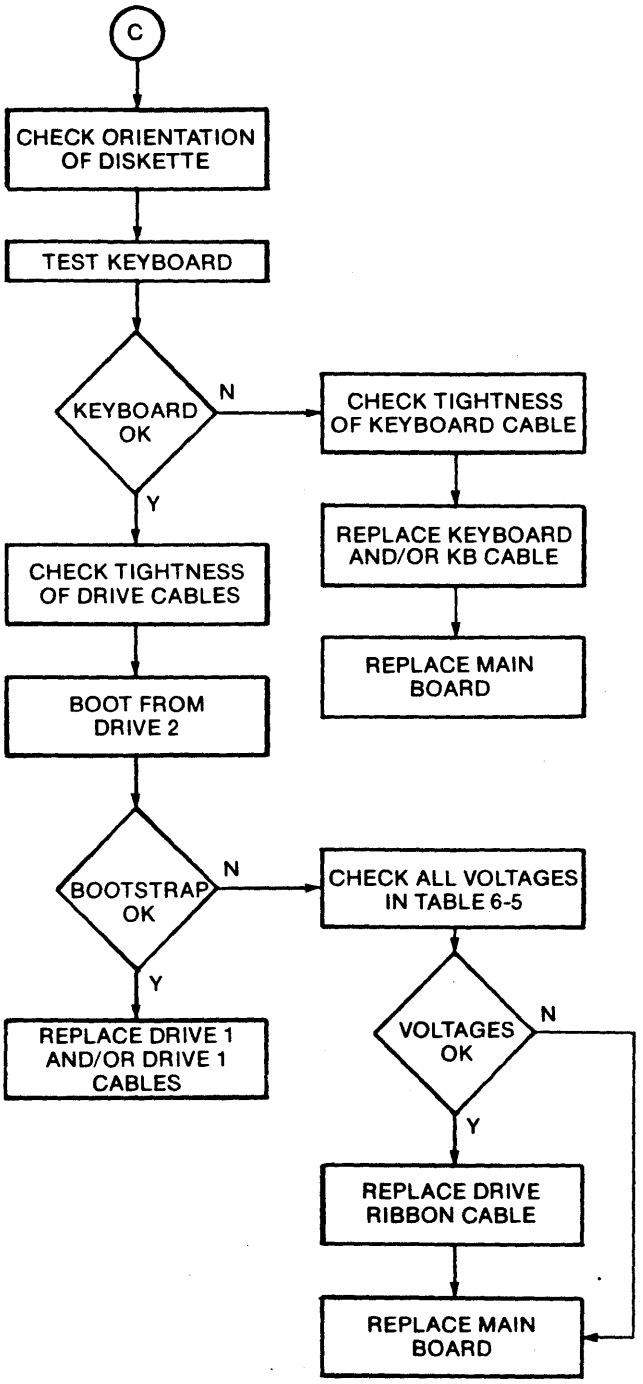


COMMENTS

F401 is a 2A miniature fuse located on the Video PCB.

WARNING
WHEN REACHING INSIDE THE VIDEO MONITOR, KEEP HANDS AWAY FROM THE RED HIGH VOLTAGE WIRE ON THE SIDE OF THE CRT. THIS WIRE CARRIES A POTENTIALLY FATAL CHARGE OF 10,000 VOLTS.

Figure 7-1 (Continued)

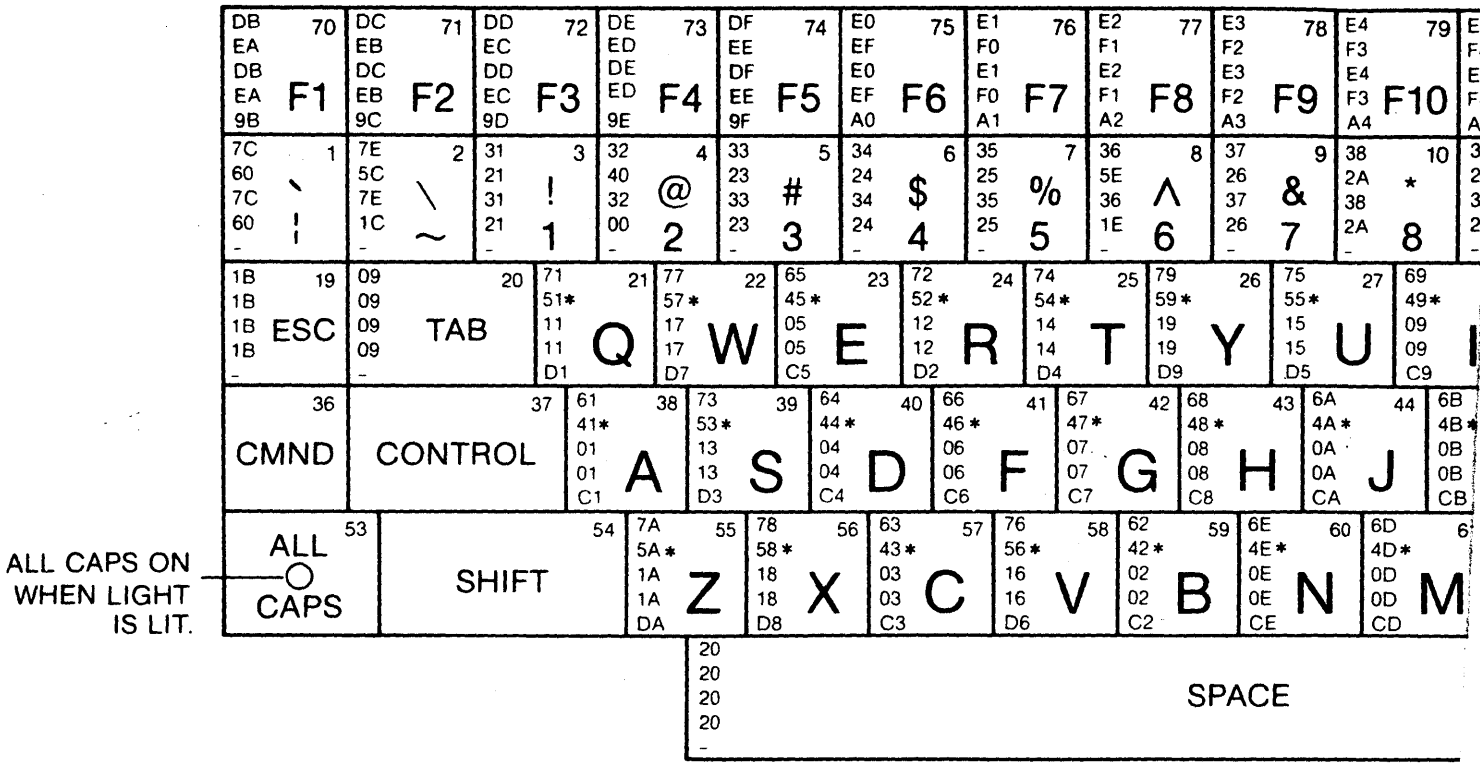


COMMENTS

To test the keyboard:

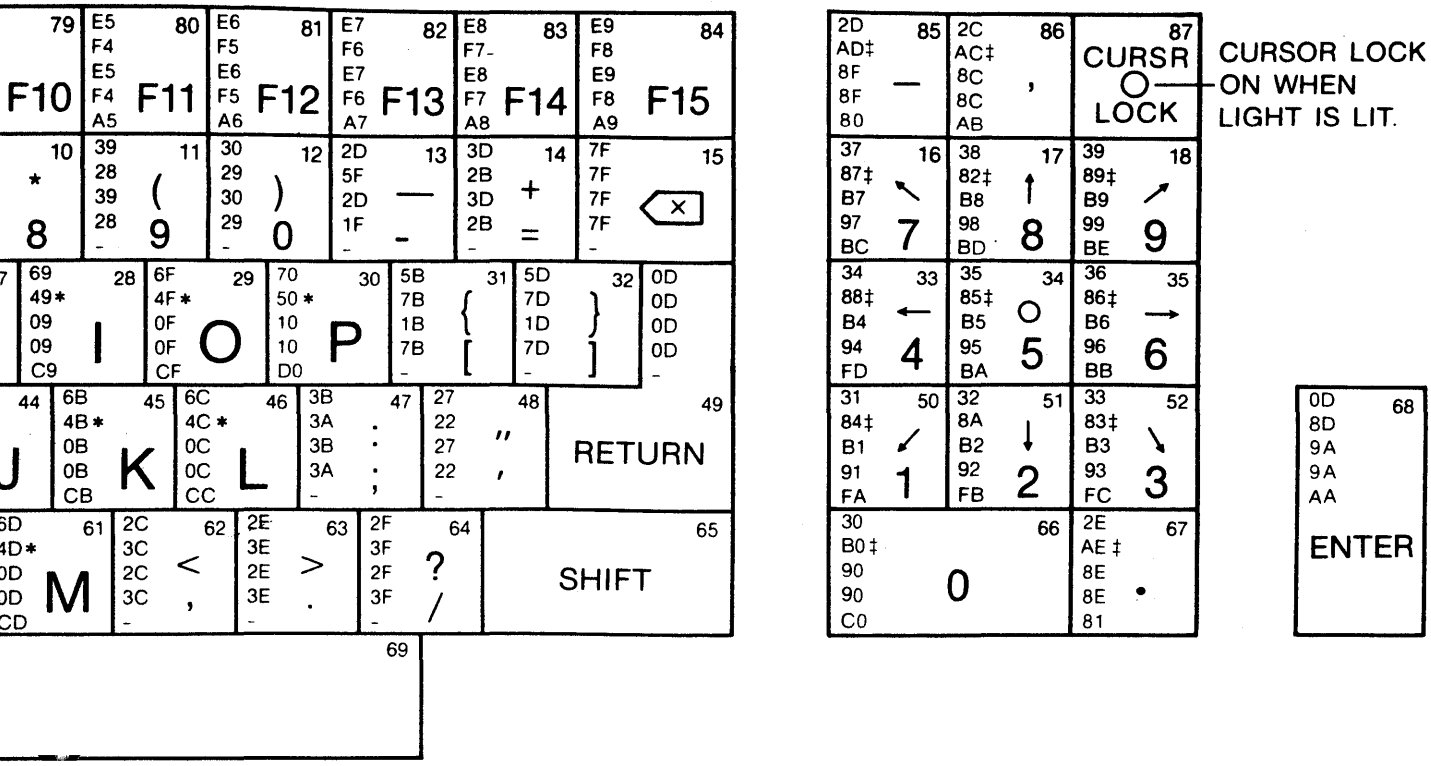
1. Check operation of the ALL CAPS key. The light in the key-cap should go on and off, alternating each time the key is pressed.
2. Press several alpha-numeric keys (except "D") one at a time. Each key should cause a "beep".

Bootstrap is succesful if screen message changes to "Integrity Test".

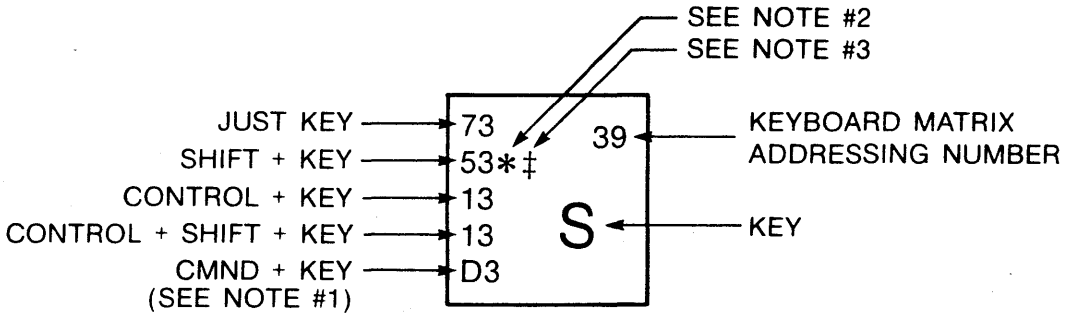


NOTES:

1. A DASH (-) IN THE 5th LOCATION MEANS IGNORE CMND KEY IF DEPRESSED. ANYTHING ELSE MEANS IGNORE SHIFT AND/OR CONTROL KEY IF DEPRESSED.
2. ONLY THOSE KEYS WITH AN ASTERISK (*) ARE AFFECTED BY THE ALL CAPS KEY. WHEN ALL CAPS IS OFF THE CODES ARE AS SHOWN. WHEN ALL CAPS IS ON THE "JUST KEY" CODE CHANGES TO THE "SHIFT + KEY" CODE.
3. ONLY THOSE KEYS WITH ‡ ARE AFFECTED BY THE CURSOR LOCK KEY. WHEN CURSOR LOCK IS OFF THE CODES ARE AS SHOWN. WHEN CURSOR LOCK IS ON THE "JUST KEY" CODES CHANGE TO THE "SHIFT + KEY" CODES.



LEGEND:



KEY.

+

SICAL LAYOUT

2. KEYBOARD ASCII CODES BY KEY

KEY	NORMAL	SHIFT	CONTROL	CONTROL/ SHIFT	CMND
Main Keyboard:					
TAB	09	09	09	09	-
RETURN	0D	0D	0D	0D	-
ESC	1B	1B	1B	1B	-
Space	20	20	20	20	-
' "	27	22	27	22	-
, <	2C	3C	2C	3C	-
- _	2D	5F	2D	1F	-
. >	2E	3E	2E	3E	-
/ ?	2F	3F	2F	3F	-
0)	30	29	30	29	-
1 !	31	21	31	21	-
2 @	32	40	32	00	-
3 #	33	23	33	23	-
4 $	34	24	34	24	-
5 %	35	25	35	25	-
6 ^	36	5E	36	1E	-
7 &	37	26	37	26	-
8 *	38	2A	38	2A	-
9 (	39	28	39	28	-
; :	3B	3A	3B	3A	-
= +	3D	2B	3D	2B	-
[{	5B	7B	1B	7B	-
] }	5D	7D	1D	7D	-
A	61	41	01	01	C1
B	62	42	02	02	C2
C	63	43	03	03	C3
D	64	44	04	04	C4
E	65	45	05	05	C5
F	66	46	06	06	C6
G	67	47	07	07	C7
H	68	48	08	08	C8
I	69	49	09	09	C9
J	6A	4A	0A	0A	CA
K	6B	4B	0B	0B	CB
L	6C	4C	0C	0C	CC
M	6D	4D	0D	0D	CD
N	6E	4E	0E	0E	CE
O	6F	4F	0F	0F	CF
P	70	50	10	10	D0
Q	71	51	11	11	D1
R	72	52	12	12	D2

KEY	NORMAL	SHIFT	CONTROL	CONTROL/ SHIFT	CMND
S	73	53	13	13	D3
T	74	54	14	14	D4
U	75	55	15	15	D5
V	76	56	16	16	D6
W	77	57	17	17	D7
X	78	58	18	18	D8
Y	79	59	19	19	D9
Z	7A	5A	1A	1A	DA
| `	7C	60	7C	60	-
~ \	7E	5C	7E	1C	-
<X]	7F	7F	7F	7F	-
F1	DB	EA	DB	EA	9B
F2	DC	EB	DC	EB	9C
F3	DD	EC	DD	EC	9D
F4	DE	ED	DE	ED	9E
F5	DF	EE	DF	EE	9F
F6	E0	EF	E0	EF	A0
F7	E1	F0	E1	F0	A1
F8	E2	F1	E2	F1	A2
F9	E3	F2	E3	F2	A3
F10	E4	F3	E4	F3	A4
F11	E5	F4	E5	F4	A5
F12	E6	F5	E6	F5	A6
F13	E7	F6	E7	F6	A7
F14	E8	F7	E8	F7	A8
F15	E9	F8	E9	F8	A9

Numeric Pad:

,	2C	AC	8C	8C	AB
-	2D	AD	8F	8F	80

KEY	NORMAL	SHIFT	CONTROL	CONTROL/ SHIFT	CMND
.	2E	AE	8E	8E	81
0	30	B0	90	90	C0
1	31	84	B1	91	FA
2	32	8A	B2	92	FB
3	33	83	B3	93	FC
4	34	88	B4	94	FD
5	35	85	B5	95	BA
6	36	86	B6	96	BB
7	37	87	B7	97	BC
8	38	82	B8	98	BD
9	39	89	B9	99	BE
Enter	0D	8D	9A	9A	AA

NOTE

* Single dash means ignore CMND key if pressed.

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